Microelectronics Journal 129 (2022) 105590

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Substrate BOX engineering to mitigate the self-heating induced degradation in nanosheet transistor

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ARTICLE INFO

Keywords:
Nanosheet transistor
Self-heating effect
Ambient temperature
Thermal contact resistance
Coupled thermodynamic
Hydrodynamic

ABSTRACT

The continued scaling of *3D* transistors into the ultra-scaled-down nanoscale regime causes self-heating effect (SHE) driven thermal deterioration. Particularly in silicon-on-insulator (SOI) FETs, the induced thermal degradation is more severe due to the presence of a conventional lower thermal conductivity material (i.e., SiO_2) as a buried oxide (BOX), which obstruct the heat flow from the active area to substrate. Thus, the lattice temperature rises above the ambient temperature. Therefore, in this paper, we proposed a substrate-BOX engineered Nanosheet (BOXNS) FET to mitigate the self-heating-induced thermal degradation. Through well-calibrated TCAD models, we investigated the impact of incorporating a superior dielectric material with significantly higher thermal conductivity, such as crystalline diamond (k_{th} = 2000 W m^{-1} K^{-1}) in place of conventional SiO_2, possessing lower thermal conductivity (k_{th} = 1.4 W m^{-1} K^{-1}) beneath the source and drain region. The results reveal that the proposed BOXNS FET effectively improves the SHE-induced thermal degradation in terms of ON current (I_{ON}), OFF current (I_{OFF}), effective thermal resistance (R_{eff}), and lattice temperature ($T_{lattice}$), compared to the conventional SiO_2 Nanosheet (SiONS) FET. In BOXNS, the hotspots from the active (channel) region find a pathway through the realized crystalline diamond (DLC) and thus decreases the lattice temperature by 13.5 K. Moreover, the dimensional variation, such as channel thickness variation in the proposed BOXNS FET, shows less effective thermal resistance and lattice temperature fluctuations than the SiONS FET while varying the ambient temperature from 300 K to 370 K.

1. Introduction

Over the last two decades, nonplanar device architectures have been widely explored, as conventional planar devices are driven by the severity of the short channel effects (SCEs) [1–3]. The nonplanar multigate devices, such as FinFETs, gate-all-around FETs (GAAFETs), nanowires (NW), etc., provide superior gate control and enhanced performances. A new edition to this era is vertically stacked Nanosheet FETs, which offer higher drivability at the same footprint area of a FinFET [4–6]. Nanosheets (NS) are being explored continuously to satisfy the pace of Moore's law and beyond for high drive current (I_{ON}), excellent current ratio (I_{ON}/I_{OFF}), power performance, and CMOS compatible fabrication flow, and suppressed SCEs compared to the conventional planar MOSFET [7–9]. Nanosheets with fully (partially) bottom dielectric isolation could be a potential candidate primarily due to subsiding leakage current, decreased parasitic capacitance, enhanced frequency response, immunity against process variation, and power performance optimization [10–12]. Despite the excellent gate electrostatics property, the nanosheets suffer from a severe heat-flux crowding issue due to the confined geometry. In nanosheet FET, the sheets (channels) are surrounded by the low thermal conductivity material that creates abysmal self-heating-induced deterioration. The accumulation of heat

and strong phonon confinement severely affects the thermal reliability of the nanosheet FET [13,14]. The severity of the arduous self-heating effects (SHEs) induced thermal degradation is especially more viable in partially bottom dielectric silicon-on-insulator (SOI) nanosheet, which is devised on a conventional buried oxide layer (i.e., SiO_2). The substrate with SiO_2 as a buried oxide (BOX) obstructs the heat flow from the active sheet area to the substrate due to the presence of lower thermal conductivity material, i.e., SiO_2 (k_{th} = 1.4 W m^{-1} K^{-1}). Moreover, the sheets (i.e., channels) in the nanosheet transistor are also wrapped by the low thermal conductivity material (i.e., SiO_2 as the gate dielectric interfacial layer), which increases the device's thermal resistance. Thus, due to enhanced phonon boundary scattering (PBS), the lattice temperature increases, leading to SHE and, in turn, device

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https://doi.org/10.1016/j.mejo.2022.105590
Received 14 August 2022; Received in revised form 16 September 2022; Accepted 18 September 2022
Available online 23 September 2022

characteristics and reliability severely affected [15]. Consequently, the self-heated lattice temperature reduces threshold voltage's transverse effect and carrier mobility degradation [16,17]. Therefore, SOI-based nanosheet structure doubly deteriorates the device performance, one due to the low thermal conductivity of the SiO_2 and the second because SHE-induced thermal degradation. Thus, we proposed a new structure, i.e., BOXNS FET, which comprises the crystalline diamond (DLC) as the alternative to the SOI concept (i.e., SiONS), in which the thermal insulator SiO_2 is replaced with the attractive diamond insulator material which is an excellent thermal conductor.

Available literature also claimed that the fabrication of DLC as a substrate is compatible with the silicon device fabrication process and could stand without degradation and cross-contamination [18–20]. Crystalline-diamond (DLC) has advantages of having higher thermal conductivity ($k_{th} = 20$ W cm^{-1} K^{-1}), high electric field breakdown (10 MV cm^{-1}), and low dielectric constant ($\epsilon_r = 5.7$) compared to other dielectric materials [21]. Thus, we proposed a fabrication-compatible BOXNS FET for reliable operation. *The key contributions are*:

(i) Proposal and investigation of a novel substrate buried oxide (BOX) engineered Nanosheet structure to mitigate the self-heating induced thermal degradation.
(ii) The results of the proposed BOXNS FET are compared with the baseline SiONS FET, i.e., having a conventional SiO_2 layer as a BOX.
(iii) The impact of varying the ambient temperature from 300 K to 370 K on various device performances has been thoroughly investigated using well-calibrated TCAD models.
(iv) The analysis of device dimensional variation, such as channel (sheet) thickness on SHE-induced thermal and electrical performance, has been performed.

The manuscript is organized as follows: Section 2 illustrates the device structure of the baseline (SiONS) and the proposed (BOXNS) FET and calibration setup against the experimental data. The self-heating effect in the proposed BOXNS and SiONS FET are discussed in Section 3, considering the varying ambient temperature and channel thickness. Finally, section 4 concludes the manuscript.

2. Device structure and simulation methodology

This section explains the device architecture and possible fabrication flow of the proposed BOXNS FET structure. In the proposed BOXNS FET, a diamond-like carbon (DLC) layer is placed beneath the source/drain (S/D) pads, as shown in Fig. 1 (b,d). We have performed an extensive TCAD simulation to analyze the impact of DLC on the device characteristics. The results are also compared with the conventional SiO_2-based SiONS FET, as shown in Fig. 1 (a,c). The S/D and the channel regions are uniformly doped, whereas the Gaussian doping is considered in the extension region to mimic the actual doping scenario. This prevents random dopant fluctuation (RDF), drain-induced barrier lowering (DIBL), and abrupt electric field breakdown [22]. The sheets (channels) are wrapped with dielectric material consisting of 0.9 nm as an effective oxide-thickness (EOT), which comprises SiO_2 as an interfacial layer (IL) of 0.6 nm thickness stacked with 1.7 nm high-k dielectric (i.e., HfO_2) [23]. In Nanosheet FET (NSFET), the sheets are vertically stacked between S/D pads; thus, the effective heat-flux path would be through the drain pad to the substrate. In the proposed BOXNS FET, the presence of DLC beneath the drain provides a pathway to heat-flux and mitigates the lattice heating. The device parameters used in our simulation are mentioned in Table 1, which are as per International Roadmap for Devices and System (IRDS) projections [24]. In Fig. 2, we have also provided the possible fabrication steps of the proposed BOXNS FET structure using a flow chart. The partially bottom dielectric isolation nanosheet FET is similar to the conventional NSFET and is compatible with the FinFET fabrication technique [12]. The stacked Si/SiGe epitaxy layer is grown as the first layer containing a high percentage of Ge layer. The ultra-high selectivity process is required to prevent erosion during the channel release, followed by the inner and outer spacer formation [12]. The bottom dielectric layer below S/D plays a vital role because this region is exposed to multiple etch processes. Here, crystalline diamond (DLC) having higher thermal conductivity is strategically placed beneath the S/D pads in the BOXNS FET to mitigate the SHE-induced thermal degradation [25], which acts as the thermal dielectric and provides the heat removal path. Replacing the partially bottom SiO_2 with the crystalline diamond is a practical step as it is compatible with the current integrated circuit fabrication technology [26]. The remote roughness scattering can be reduced by utilizing various bonding approaches [27]. Si_3N_4 is used as the spacer to assuage the gate-source/drain fringing capacitance, and TiN is used as a gate electrode.

Table 1
Parameter table.

Device Parameter	Value
Channel Thickness (t_{CH})	4 nm–7 nm
Channel Width (t_w)	25–58 nm
Channel Length (L_G)	12 nm
Spacer Length (L_{sp})	5 nm
Interfacial EOT (T_{EOT})	0.9
Spacer Dielectric (k)	7.5
Sheet Spacing (T_{sheet})	11 nm
Source/Drain Doping	2×10^{20} cm^{-3}
Channel Doping	1×10^{16} cm^{-3}
Substrate Doping	1×10^{18} cm^{-3}
S/D Metal-Si Interface Resistance	8.4×10^{-10} Ωcm^2

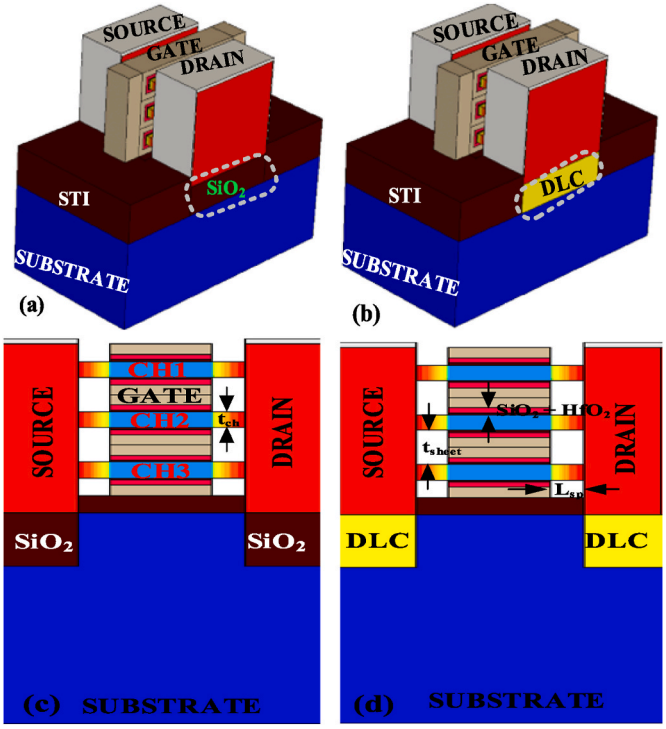

Fig. 1. (a–b) *3D* schematic of the buried SiO_2 Nanosheet (SiONS) FET and buried DLC BOXNS FET beneath the source/drain region; (c) 2*D* cross-sectional structure for fair comparison of vertically stacked nanosheet transistor with SiO_2 as a buried oxide layer beneath S/D pads; (d) *2D* cross-sectional view of the proposed vertically stacked BOXNS FET comprises DLC instead of SiO_2. The crystalline diamond (DLC) is strategically placed under the source/drain (S/D) region to subside the leakage current and SHE.

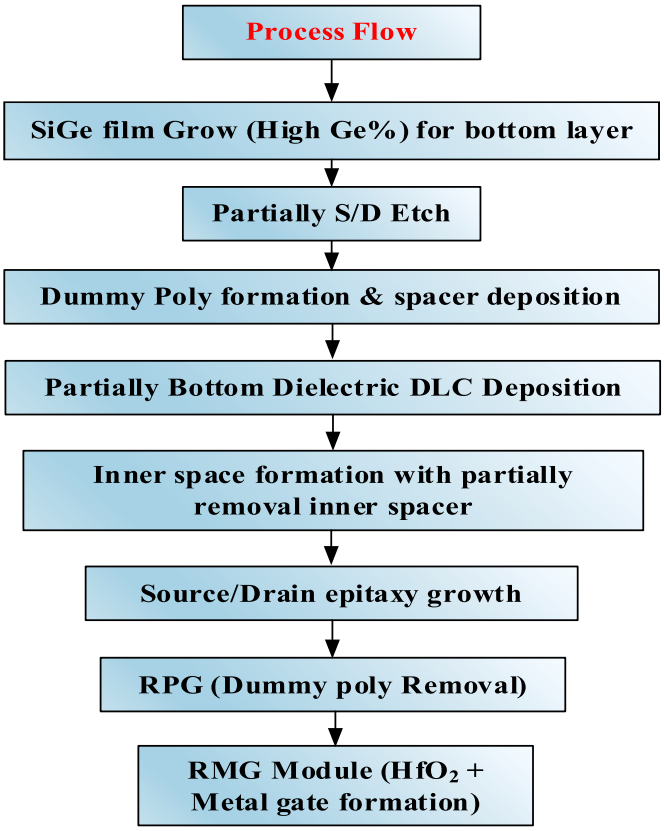

Fig. 2. The possible fabrication flow of the partial bottom Silicon on diamond nanosheet (BOXNS) FET and partially bottom Silicon on insulator (SiONS) nanosheet transistor.

- **TCAD Calibration:**

A vertically stacked nanosheet with substrate engineered BOX layer, i.e., BOXNS FET, is realized using Sentaurus TCAD [28]. The models employed in the TCAD setup are well-tuned and calibrated against the experimental data [7]. The density gradient model is invoked to capture the channel.

spatial and electrostatic quantum confinement. To capture the carrier distribution near the oxide/silicon interface, the modified local density approximation model (MLDA) is included. Further, the ballistic, vertical field, and high field saturation models are incorporated to consider the impact of short channel effects (SCEs) [29]. The inversion and accumulation layer (IAL) mobility models have been included to assess the mobility deterioration caused by surface roughness scattering, phonon scattering, and Coulomb scattering. The Slotboom model was employed to capture the doping/temperature-dependent bandgap narrowing. The Shockley-Read-Hall (SRH) model is used to study the cumulative effect of carrier generation and recombination. Finally, the work function of the TiN is tuned to the permissible limit to match the simulated and experimental transfer characteristics (I_{DS}-V_{GS}), as shown in Fig. 3. In general, the thermal conductivity (k_{th}) of the channel is decreased due to surface phonon scattering [30]. The thermal conductivity (k_{th}) of the Silicon depends on the lattice temperature ($T_{lattice}$), channel thickness (t_{CH}), doping (N_d), and the mole fraction (x), as follows [31]:

$$k = \frac{1}{3} \times \frac{1}{2\pi^x} \times n_j \times \sum_j \int_0^{\omega_{0j}} \frac{\tau_{\omega,j}}{\nu_{\omega,j}} C(\omega)\omega^2 d\omega \tag{1}$$

$$C(x) = kx^2 e^x (e^x - 1)^{-2} \tag{2}$$

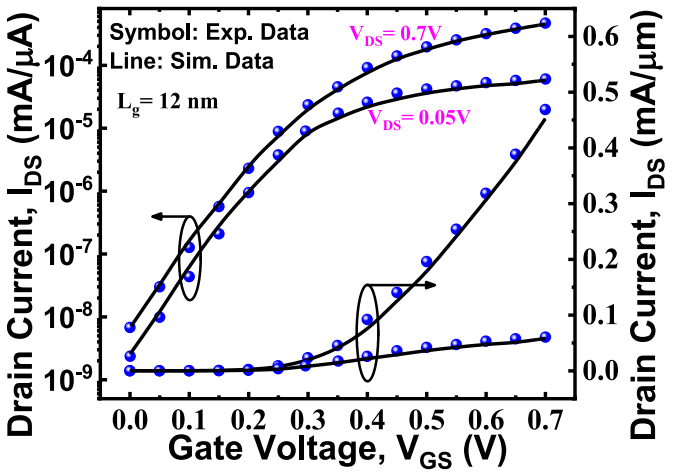

Fig. 3. TCAD Calibration against the experimental data [7], showing a good match in I_{DS}-V_{GS} (transfer characteristics) data.

$$x = \hbar\omega/kT \tag{3}$$

Here, $\nu_{\omega,j}$ and ω_{0j} denotes the velocity and maximum frequency, respectively. $\tau_{0,j}$ represents the total relaxation time. In our simulation, the interface thermal contact resistance is considered as 4×10^{-5} cm^2K/W [32–35]. Fig. 4 shows a comparative bar chart of the thermal conductivities of different materials used in our simulation. Not to mention otherwise, in our TCAD simulation, drift-diffusion along with lattice heat flow equations are used to capture the self-heating effect in the NSFET. The energy balance equations from the hydrodynamic model are used to calculate the heat flux.

3. Results and discussion

In this section, we discuss the self-heating-induced performance evaluation and the impact of ambient temperature on the device characteristics of the SiONS and BOXNS FET. The impact of the device geometry variation is also investigated. The section is divided into the following sub-sections:

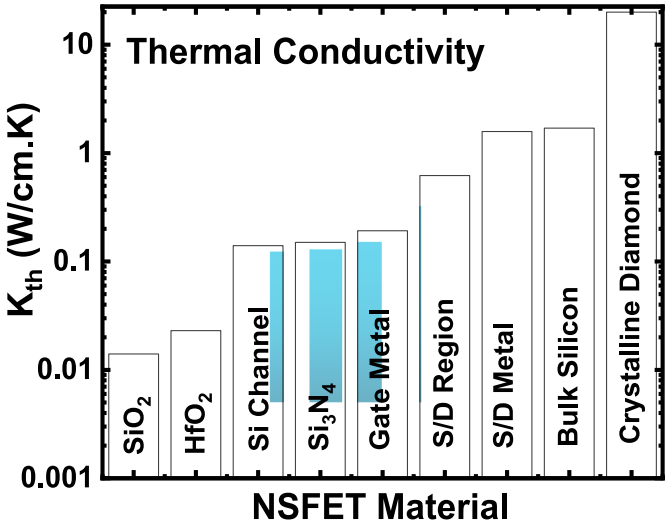

Fig. 4. Shows the thermal conductivity values of the materials used to fabricate nanosheet FET.

3.1. Device performance evaluation under SHE

This subsection deals with the electrical characteristic of the proposed BOXNS FET and SiONS FET under the consideration of the self-heating effect (SHE) induced thermal degradation. The impact of the SHE-induced thermal degradation is evaluated in terms of ON current (I_{ON}) degradation of the SiONS FET compared to the BOXNS FET to analyze the severity of the SHE. Fig. 5 shows the impact of the SHE on the transfer characteristics of both the BOXNS and SiONS FET. A small peak (0.8%) current degradation is observed in BOXNS FET due to surface roughness scattering at the silicon-diamond interface [27]. Due to SHE, heat accumulation occurs in the active (channel/sheet) region and degrades the I_{ON}, increasing the lattice temperature. Thus, the device performance to its zenith values decreases. We observed that I_{ON} is degraded by ~7.65%, and lattice temperature is enhanced to 58.2 K at room temperature (300 K) in SiONS FET. However, using the crystalline diamond beneath the S/D pads in the BOXNS FET, the I_{ON} is improved by ~2.8%, and the lattice temperature is enhanced to 13.8 K. This is due to the decrease in heat accumulation in the active (channel/sheet) region at the drain side and shifting the heat flow path towards the substrate compared to SiONS FET. Fig. 6 shows the spatial variation of the lattice temperature along the channel direction. The maximum value of the hotspot of lattice temperature is observed at the channel and drain junction. The high-energy electrons move under the influence of a high electric field from the source region scattered heavily with the optical phonons and transfer their joule and carrier energy (kinetic energy) and undergo energy relaxation at the drain side, which results in enhanced lattice temperature. However, the lattice temperature difference between channel-1 (CH1) to channel-3 (CH3) is 7.2 K in BOXNS FET compared to the SiONS FET at the drain side due to heat energy dissipated towards the substrate.

3.2. Impact of ambient temperature on BOXNS and SiONS FET

The performance characteristics of electronic devices are significantly affected by ambient temperature. Fig. 7 shows the impact of varying the temperature on the electrical (I_{ON} and I_{OFF}) and thermal characteristics ($T_{lattice}$ and $R_{effective}$) of the BOXNS and SiONS FET, respectively. As the temperature increases from room temperature to 370 K, the lattice temperature ($T_{lattice}$) increases from 358.2 K to 420 K (17.32%) in SiONS FET. Due to this, the effective thermal resistance increases by ~8.47%, which results in ON current degradation from 290 μA to 280 μA (~8.72%) and 10.4 times enhancement in leakage current.

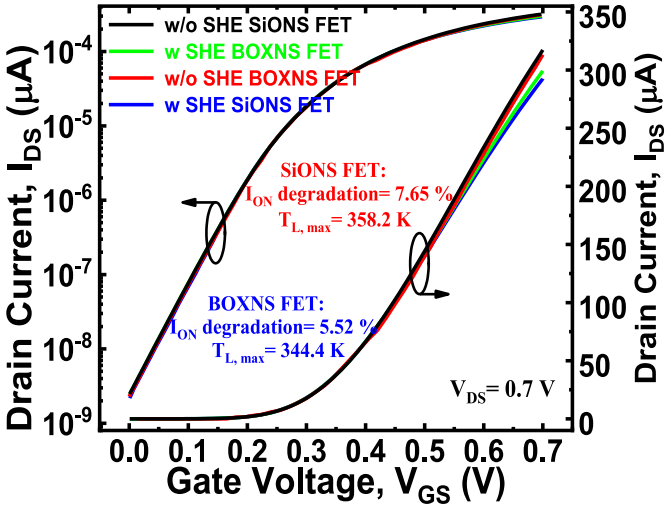

Fig. 5. Shows the transfer characteristics (I_{DS}-V_{GS}) of NSFET with partially depleted silicon on the insulator (SiONS) and proposed silicon on the diamond (BOXNS) with and without a self-heating effect.

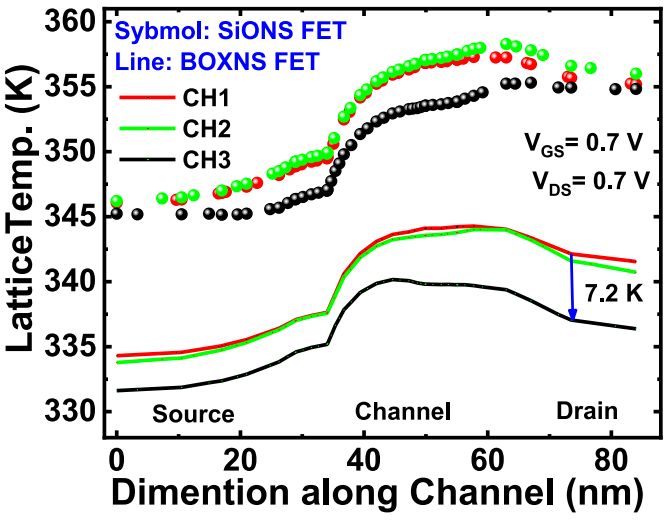

Fig. 6. Shows the variation of the lattice temperature along the channel. While strategically placing the DLC beneath the S/D region, the BOXNS FET lowers the lattice temperature. Also, the difference between the lattice temperature variation in CH1 and CH3 is increased in BOXNS FET due to a change in the effective heat flow path (hotspot) towards the substrate region.

However, using the DLC as a BOX layer in BOXNS FET, the effective heat flux shifted from the device active (channel/sheet) region towards the substrate (Fig. 6), which resulted in 3.83% and 28.12% improvement in $T_{lattice}$ and $R_{effective}$, respectively.

Therefore, the ON current is improved by 2.8% compared to SiONS FET. The variation in ambient temperature severely affects the threshold voltage shift and can be measured by using the $\Delta V_{th}/\Delta T$ [36]. When ambient temperature increases from 300 K to 370 K, the observed threshold voltage coefficient is −0.525 mV/K for SiONS FET and −0.518 mV/K for BOXNS FET, which proves the higher thermal reliability of the BOXNS FET compared to the SiONS FET. The OFF current in both devices is almost similar (Fig. 7b) due to less scattering occurring in the channel region at lower gate voltage. The effect of SHE-induced degradation is more at higher ambient temperatures in SiONS FET than BOXNS FET, as shown in Fig. 8. At higher temperatures, the thermal conductivity is reduced, resulting in more heat accumulation in the device, and current decreases steadily in SiONS FET. However, using a higher thermal conductivity material releases the accumulated heat towards the substrate; thus, SHE is less pronounced in BOXNS FET. The change in drain current and lattice temperature is calculated as mentioned in Eqs. (4) and (5) [37,38]:

$$\Delta I_{ON} = \frac{I_{L,w/o\ SHE} - I_{L\ w\ SHE}}{I_{L,\ w/o\ \ SHE}} \times 100\ \% \tag{4}$$

$$\Delta T_{Lattice} = \frac{T_{L,Max} - T_A}{T_{Amb}} \times 100\ \% \tag{5}$$

where $I_{L,\ w\ SHE}$, and $I_{L,\ w/o\ SHE}$ is the drain current with and without self-heating effect, and $T_{L,\ Max}$ is maximum lattice temperature with SHE consideration.

3.3. Impact of channel thickness

The variation in device geometry significantly affects the electrical and thermal characteristics due to the change in gate controllability and mobility of the device. Therefore, the impact of varying the channel thickness (T_{CH}) while varying the ambient temperature of the NSFET is necessary to get a deeper detailed insight into the self-heating effect-induced thermal degradation. Fig. 9 shows the variation in T_{CH} from 4 nm to 7 nm and its impact on the parameters such as lattice temperature, effective thermal resistance, and lattice heat flux. However, by

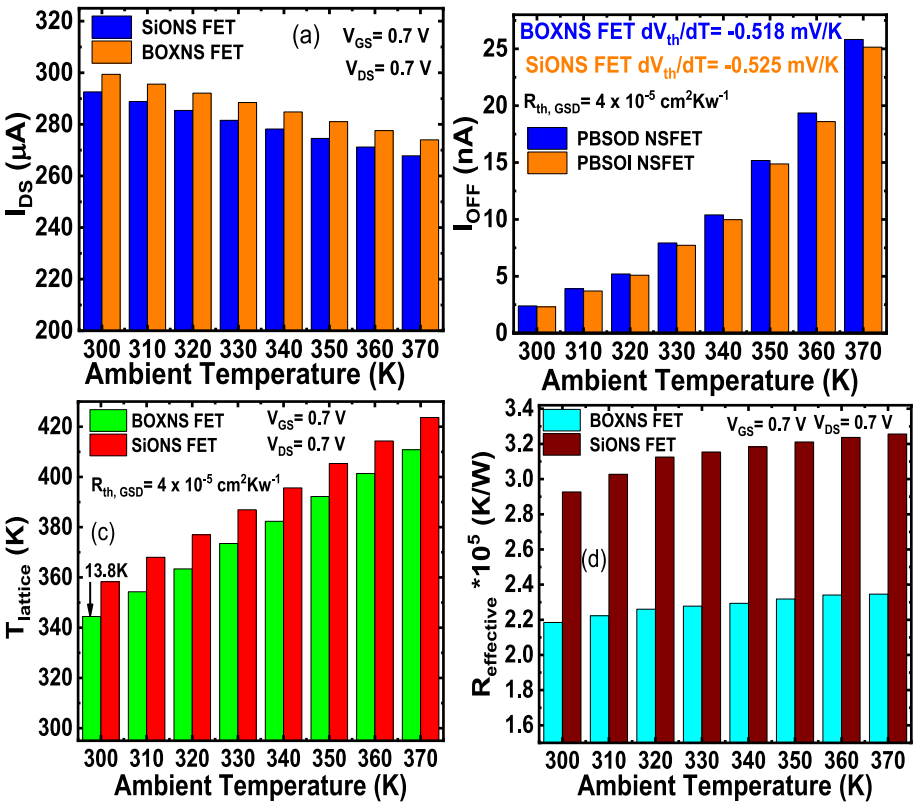

Fig. 7. Shows the impact of varying the temperature on device electrical (I_{ON} and I_{OFF}) and thermal characteristics ($T_{lattice}$ and $R_{effective}$) of SiONS and BOXNS FET.

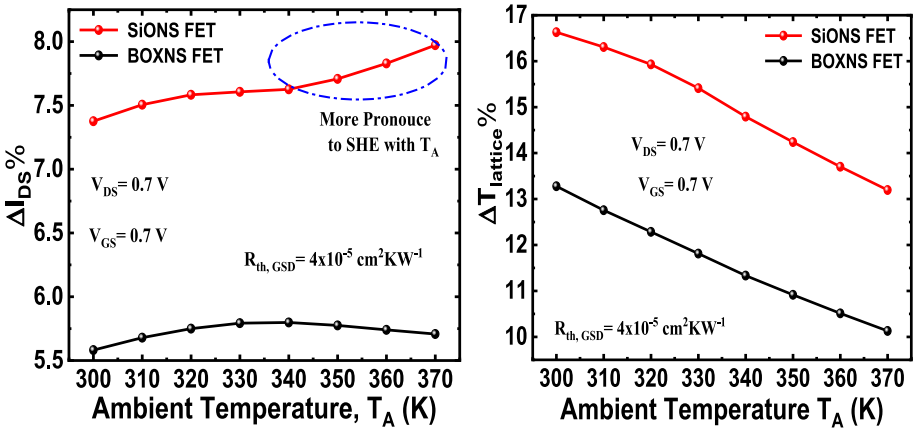

Fig. 8. The impact of ambient temperature on the effective change in drain current (ΔI_{DS}) and lattice temperature ($\Delta T_{lattice}$). The fluctuation in ΔI_{DS} and $\Delta T_{lattice}$ is less pronounced in BOXNS FET due to the uniform distribution of lattice temperature.

increasing the channel thickness increases the surface-to-volume ratio, which increases the inversion charge density and causes an increase in the drain current. Moreover, the increase in ambient temperature reduces carrier mobility, which results in a decrease in drain current.

However, this I_{ON} degradation can be mitigated using BOXNS FET (Fig. 9a). With an increase in T_{CH}. In the BOXNS structure with increasing T_{CH}, the primary heat dissipation path increases, which increases the lattice heat flux (Fig. 9b) and lattice temperature of the device (Fig. 9c). Increasing the channel thickness enhances the circumference of the device; however, the thermal heat conductivity of the device stagnates, suggesting that higher channel thickness prevents the continuous enhancement of the lattice temperature and effective thermal resistance; thus, improved thermal reliability of the device is obtained. However, due to the use of crystalline diamond, the primary heat path in SiONS FET is altered from the device active (channel/sheet) region towards the substrate in BOXNS FET. Thus, the acquired results show that proper consideration of device dimension and substrate material can mitigate the self-heating effect in Nanosheet FET.

4. Conclusions

Using well-calibrated TCAD models, we have proposed a new BOXNS FET comprising the crystalline diamond beneath the drain and source regions, helping to mitigate the self-heating-induced thermal degradation. We evaluated the performance of the proposed BOXNS FET in comparison to the conventional SiO_2 layer-based NSFET, i.e., SiONS FET. The crystalline diamond having a heat thermal conductivity (~1000 times higher than SiO_2) is employed, which leads to the removal

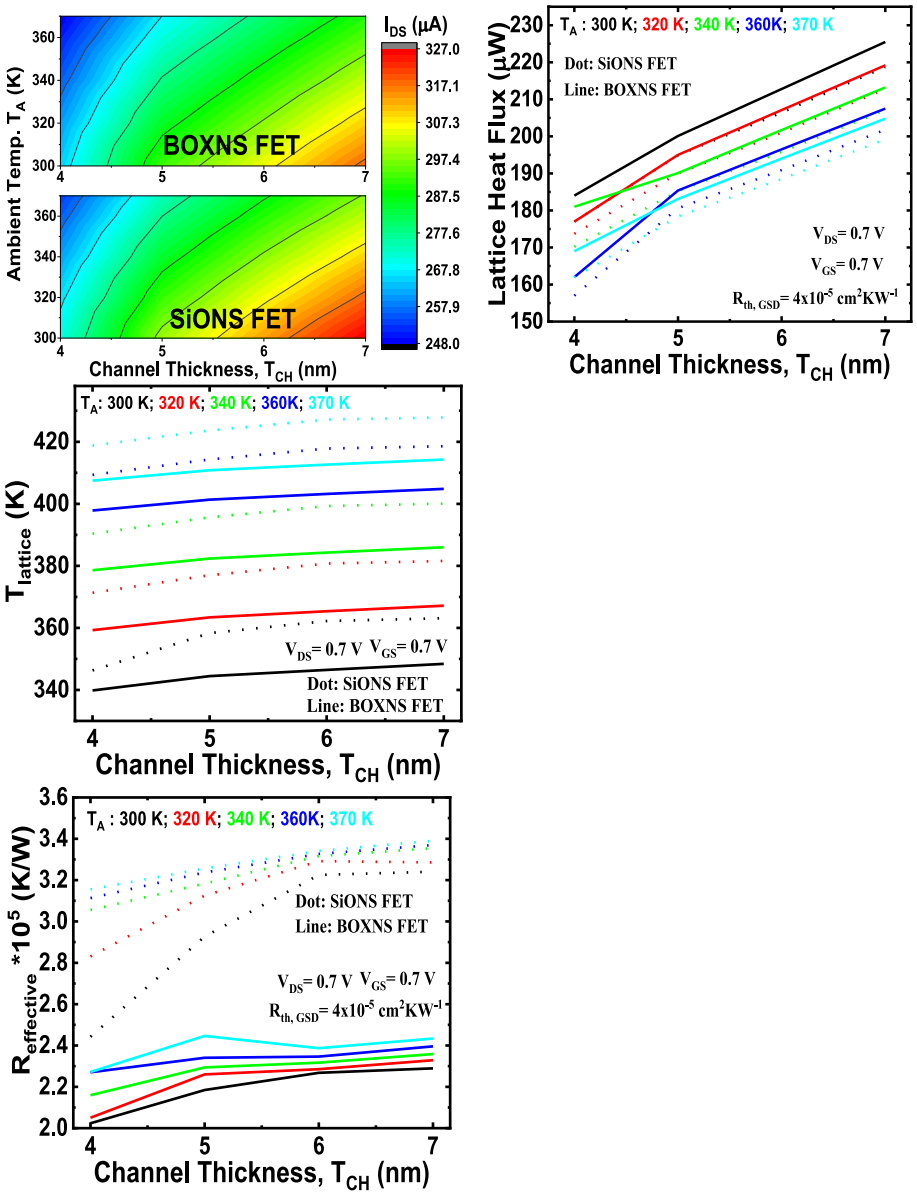

Fig. 9. Impact of increasing the channel thickness and ambient temperature on (a) drain current variation in contour plot, (b) lattice heat flux, (c) lattice temperature, and (d) effective thermal resistance. Steadily increasing the channel thickness of the NSFET enhance the lattice heat flux, which enhances the lattice temperature and effective thermal resistance of the device. However, the drain current of the device increases due to enhancement in inversion charge particles with the enhanced surface-to-volume ratio.

of the hotspot towards the substrate. Thus, it enhances the heat removal capability and allows the uniform distribution of the lattice temperature in the device's active (channel) regions. Therefore, by increasing the ambient temperature from 300 K to 370 K, the average rise in the device lattice temperature is improved by 13.8 K, and device thermal resistance is decreased by 28.12%. This results in approximately ~2.8% improvement in the I_{ON} in BOXNS FET compared to SiONS FET. Further, we have also investigated the impact of varying channel thickness on device performance. As the sheet thickness increases from 4 nm to 7 nm, the surface-to-volume ratio increases the heat dissipation path, which enhances the lattice temperature, lattice heat flux, and effective thermal resistance. However, due to the use of crystalline diamond, the severity of SHE-induced thermal degradation is less affected, and lattice temperature, lattice heat flux, and effective thermal resistance are improved by 25.8%, 42%, and 50.2% in BOXNS FET compared to SiONS FET. Therefore, the proposed BOXNS FET can be a promising candidate for high-volume production and energy-efficient future FET devices due to overcoming the power accumulation constraints in electronics.

Author statement

Sunil Rathore: Conceptualization, Methodology, Data curation, Software, Writing – original draft preparation, Investigation. **Rajeewa Kumar Jaisawal**: Conceptualization, Methodology, Investigation, Software. **Navneet Gandhi**: Conceptualization, Methodology, Investigation. **P. N. Kondekar**: Supervision, Visualization. **Navjeet Bagga**: Supervision, Writing- Reviewing and Editing, Corresponding Author, Conceptualization, Visualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

Acknowledgment

N. Bagga greatly acknowledged the support received from the PDPM IIITDM Jabalpur, project title "Design and Performance Investigation of Negative Capacitance Tunnel Field Effect Transistor for Digital/Analog Applications," project no.IIITDMJ/ODRSPC/2022/88.

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