PAPER

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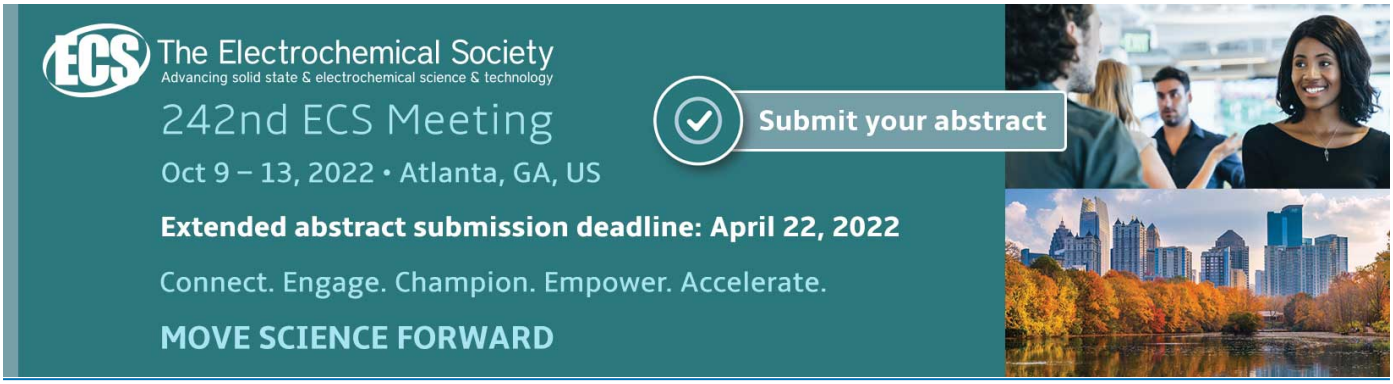

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Investigation of ambient temperature and thermal contact resistance induced self-heating effects in nanosheet FET

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Abstract

Self-heating effect (SHE) is a severe issue in advanced nano-scaled devices such as stacked nanosheet field-effect transistors (NS-FET), which raises the device temperature (T_D), that ultimately affects the key electrical characteristics, i.e. threshold voltage (V_T), DIBL, subthreshold slope (SS), I_{OFF}, I_{ON}, etc. SHE puts design constraints in the advanced CMOS logic devices and circuits. In this paper, we thoroughly investigated the impact of ambient temperature and interface thermal contact resistance induced-self heating effect in the NS-FET using extensive numerical simulations. The weak electron–phonon coupling, phonon scattering, and the ambient temperature-induced joule energy directly coupled with thermal contact resistance cause the SHE-induced thermal degradation, which increases the device temperature (T_D) and affects the device reliability. The baseline NS-FET is well-calibrated with the experimental data and *3D* quantum corrected drift-diffusion coupled hydrodynamic and thermodynamic transport models is used in our TCAD framework to estimate the impact of ambient temperature and interface thermal contact resistance on the device performance. Moreover, we also evaluate the SHE-induced performance comparison of NS-FET with conventional FinFET and found that thermal degradation in NS-FET potentially worsen the electrical characteristics. Thus, a detailed TCAD analysis shows that the ambient temperature and interface thermal contact resistances deteriorate the effective thermal resistance (R_{eff}) and device performance metrics.

Keywords: nanosheet transistor, self-heating effect, ambient temperature, thermal contact resistance, coupled thermodynamic, hydrodynamic

(Some figures may appear in colour only in the online journal)

1. Introduction

The semiconductor industry is continuously scaling the field-effect transistors (FETs) dimension to satisfy the incessant need for high computing and low power consuming devices such as smartphones, and neuromorphic computing [1–3]. The downscaled FETs geometry is continuously evolving from planar MOSFET to nonplanar FinFET [4–6], to gate-all-around (GAA) nanowire, and stacked nanosheet FET (NS-FET) [7] for better and improved gate controllability of the structure. The thermal management of the shrinking FETs is an arduous concern due to the self-heating effect (SHE) observed in gate surrounded structures like FinFET,

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nanowire [8], and NS-FET [9], which will increase device temperature [10]. This will lead toward current degradation and several other thermal reliability problems like hot carrier injection, time-dependent dielectric breakdown, and chip lifetime reduction [11]. SHE in NS-FET has a very severe effect as compared to other MOSFETs due to the low thermal conductivity gate dielectric channel surrounding its intrinsic confined geometry. Intuitively, it is a technological challenge for the semiconductor industry to eradicate the SHE in CMOS nanoscale NS-FET devices. Many research group has worked to alleviate the SHEs in nanoscale MOSFETs [12–17]. Hetero interfacial thermal resistance (HITR) due to weak electron–phonon interaction and phonon scattering at the hetero-interface which will enhance the SHE and the drive current will be degraded further. The HITR impact on SiO_2/Si at gate-oxide/channel interface has a lower impact compared to Si/Mo at the back end of line and front end of line (BEOL/FEOL) [12]. In a highly scaled channel due to low heat dissipation, the device and circuit performance deteriorate caused by the SHE [13]. With the proper optimization of nanosheet thickness and stack spacing, a tradeoff between thermal effect (SHE, thermal crosstalk, and nonuniform temperature distribution) and electrical performance can be achieved in a three-stacked vertically NS-FET [14]. The ballistic phonon is observed at low temperature and ordinary temperature when the resistive phonon process dominates over the normal phonon process [18, 19]. The ballistic heat transport in thin films would occur in the form of large reductions in thermal conductivity compared to the bulk values in the sub-7 nm regime. The lateral thermal conductivity of the thin silicon layer decreases as the thickness of the film is reduced. The thermal effects can be mitigated by properly optimizing the device and its multiple array layout designs by considering the dependence of thermal conductivity on temperature and silicon thickness in the presence of anisotropy in nanosheet FETs [15]. The SHEs of PMOS is comparatively severe than NMOS due to its wider channel width which will cause V_T mismatch and can be mitigated by using shorter nanosheet width, longer pitch, and less number of channels [16]. These mentioned nanoscale CMOS devices' SHEs are dependent on interface thermal contact resistance ($R_{th,DSG}$) and distributed thermal resistance ($R_{th,Dist}$) which are closely related to many factors, such as interface, electrode material, and contact dimension. The quantitative estimated value of $R_{th,DSG}$ have been calculated in the range of 10^{-5}–10^{-3} cm^2 K W^{-1} by the research group based on simulations and experimental results [20–23].

1.1. Our key contribution

Firstly, a proper TCAD calibration is performed with the industry-standard stacked nanosheet FET to match the simulation data with the experimental data. Our simulation framework has incorporated all the appropriate models to capture conventional carrier flow through drift-diffusion (DD)coupled with hydrodynamic (HD) and thermodynamic (TD) transport models to include the SHE induced thermal degradation. Later, we investigated the device performance on the below points:

- Computational investigation of the carrier temperature (T_e) and device temperature (T_D) for electrothermal (ET) behavior of NS-FET.
- In addition to analyzing the device's intrinsic thermal characteristics, the effect of ambient temperature (T_A) induced SHE have also been studied. This increases the device temperature (T_D) and ultimately deteriorates the electrical characteristics of the NS-FET.
- Investigation of the impact of varying the gate, drain, and source electrode interface-thermal contact resistances ($R_{th,DSG}$) on SHE-induced electrical and thermal performance of NS-FET.

This paper aims to computationally investigate the carrier temperature (T_e) and device temperature (T_D) for ET behavior of the stacked NS-FET. We have investigated the effect of the terminal electrode's interface thermal contact resistance ($R_{th,DSG}$) and ambient temperature (T_A) induced SHEs which is the root cause of performance degradation of NS-FET. The remaining paper is organized as follows: section 2 deals with the NS-FET device structure and its calibration setup. In the simulation framework, different carrier transport models [HD and TH] are used to simulate the three-stacked NS-FET. Section 3 analyzes the SHE-induced thermal degradation and impact on electrical characteristics performance parameters such as I_{ON}/I_{OFF} ratio, drain induced barrier lowering (DIBL), and SS while varying the ambient temperature and interface thermal contact resistance of NS-FET. Finally, a conclusion is presented in section 4.

2. Device structure and simulation methodology

The *3D* isometric schematic of the three-stacked NS-FET is shown in figure 1(a). The various device design parameters used in our simulations are mentioned in table 1. The NS-FET channel is doped with 1×10^{16} cm^{-3} boron doping concentration. The source/drain is heavily doped with 2×10^{20} cm^{-3} arsenic doping concentration, and the silicon substrate is 1×10^{18} cm^{-3} highly doped to mitigate I_{OFF} and DIBL [24]. Figures 1(b) and (c) shows the *2D* view of the NS-FET in the channel direction and perpendicular to the channel direction. The source and drain contact resistance ($R_C = 8.4 \times 10^{-10}$ Ω cm^2) of the NS-FET severely affects the device's ON-resistance [25]. Titanium nitride (TiN) is selected as a gate electrode due to its engineered work function properties and Tungsten (W) is used as the source and drain electrode material in this simulation [26, 27]. The spatial quantum confinement and electrostatic phenomenon is addressed by incorporating models like modified local density approximation (MLDA) in the NS-FET. MLDA also ensures the inclusion of volume inversion charge density created due to nanosheet quantum confinement. Inversion accumulation layer mobility, high-field saturation, and thin-layer mobility model are included in this simulation to capture the exact behavior of the carrier mobility [28]. Lombardi model is included to address the mobility degradation like the remote Coulomb scattering, remote dipole scattering,

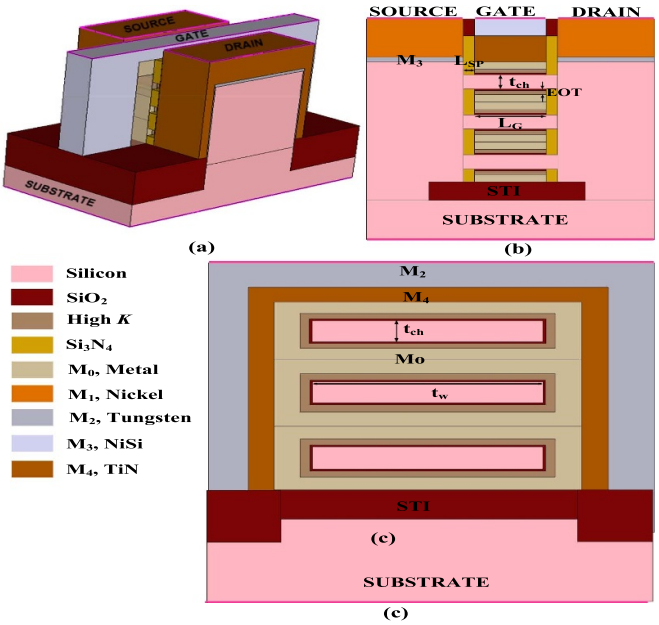

Figure 1. (a) Three-dimensional (*3D*) isometric schematic of stacked vertically NS-FET; (b) *2D* cross-section view; (c) *2D* view perpendicular to the channel direction with device design parameters are mentioned in table 1.

and remote phonon scattering occurred due to high-k gate dielectric [29]. Shockley–Read–Hall model is used to consider the generation and recombination of charge carriers. The models are incorporated in the *Sentaurus* TCAD simulator with appropriate tuned parameters to obtain reliable results [30]. Figure 2 shows a well-calibrated transfer characteristic of the baseline NS-FET with the experimental results for the lower drain voltage ($V_{DS} = 0.05$ V) and higher drain voltage ($V_{DS} = 0.7$ V) [7]. To match the transfer characteristics metal gate work function, source/drain lumped series resistance, and for the linear regime, low-field ballistic mobility parameter and saturation regime saturation velocity (v_{sat}) and high-field saturation parameters are tuned in appropriate limits. Generally, in the nanoscale regime, the phonon mean free path is restricted by the phonon-boundary scattering responsible for reducing the thermal conductivity of the nonplanar nanoscale devices [31, 32]. The thermal conductivity (k) of Si-based nanoscale devices is temperature and thickness dependent [33]. In our simulation for NSFET with thickness h, the scattering of acoustic phonons at the boundary interface reduces the mean free path, and mass fluctuation scattering occurs due to phonon-dopant impurity [34]. Thus, the thermal conductivity (k) of the Si material is given as [35]:

$$k(z) = \int_0^{\frac{\pi}{2}} \sin^3\theta \left\{ 1 - \left(\frac{h}{2\lambda(T)\cos\theta} \right) * \cos h \left(\frac{h - 2z}{2\lambda(T)\cos\theta} \right) \right\} d\theta \quad (1)$$

Table 1. Device parameters.

Device Parameter	Value
Gate Length (L_G)	12 nm
Channel Width (t_w)	25–58 nm
Channel Thickness (t_{ch})	5 nm
Spacer Length (L_{sp})	5 nm
Interfacial EOT (T_{EOT})	0.9
Spacer Dielectric (k)	4
Source/Drain Doping	2×10^{20} cm^{-3}
Channel Doping	1×10^{16} cm^{-3}
Bulk Doping	1×10^{18} cm^{-3}
Drain/Source Metal Interface Resistance	8.4×10^{-10} Ω cm^2
Thermal Properties	
Gate Metal Conductivity	0.192 W K^{-1} cm^{-1}
Drain/Source Metal Thermal Conductivity	1.7 W K^{-1} cm^{-1}
Channel Region Thermal Conductivity	0.14 W K^{-1} cm^{-1}
Drain/Source Region Thermal Conductivity	0.62 W K^{-1} cm^{-1}
Oxide Thermal Conductivity	0.014 W K^{-1} cm^{-1}
High-k Thermal Conductivity	0.023 W K^{-1} cm^{-1}
Silicon Nitride Thermal Conductivity	0.15 W K^{-1} cm^{-1}

$$\lambda(T) = \lambda_0 \frac{300}{T} \text{ nm} \quad (2)$$

$$k_0(T) = \frac{1}{a + bT + cT^2} \text{ W m}^{-1}\text{K}^{-1} \quad (3)$$

where $a = 0.03$ K m W^{-1}, $b = 1.56 \times 10^{-3}$ K^2 m W^{-1}, and $c = 1.65 \times 10^{-6}$ K^3 m W^{-1}. We assumed that the z-axis is perpendicular to the thin film of the semiconductor, λ is temperature-dependent [36], and λ_0 is 300 nm at room temperature 300 K [37]. $k_0(T)$ is the temperature-dependent thermal conductivity. We have considered the anisotropic thermal conductivity by tensors mathematical expression (k_x, k_y, k_y). The thermal conductivity values of the Si material for source/drain and channel used in our simulations are 0.62 and 0.14 W K^{-1} cm^{-1}, respectively. Intuitively, these values are two orders of a decade lower than the bulk Si thermal conductivity [38]. The DD carrier transport model along with the coupled HD and TH models are used to govern the underlying physics for analyzing the SHE-induced thermal degradation.

3. Results and discussion

The contour plot of charge density at $V_{GS} = V_{DS} = 0.7$ V is shown in figure 3(a). Figure 3(b) shows the charge density across the three-stacked vertically NS-FET line plot (ZZ') having a peak inversion charge density of 1.53×10^{19}, 1.49×10^{19}, and 1.48×10^{19} cm^{-3}, respectively. The peak inversion charge density is located in the middle of the channel due to the presence of strong electrostatic *2D* confinement of the NS-FET. The maximum charge density is found in channel-1 (ch1) and follows the trend of ch1 > ch2 > ch3, as channel-3 (ch3) is far from the source/drain contact, which has more source/drain resistance. Therefore, the peak current density decreases in ch-3.

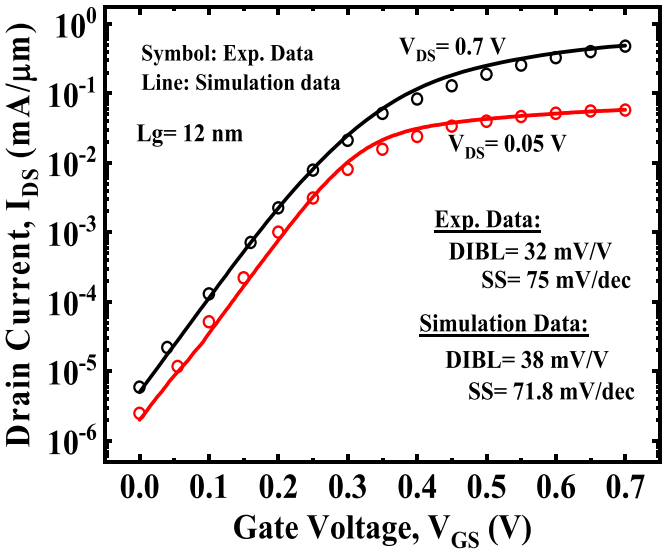

Figure 2. Calibration of the transfer characteristics with the experimentally reported NS-FET data [7] for low and high V_{DS} values.

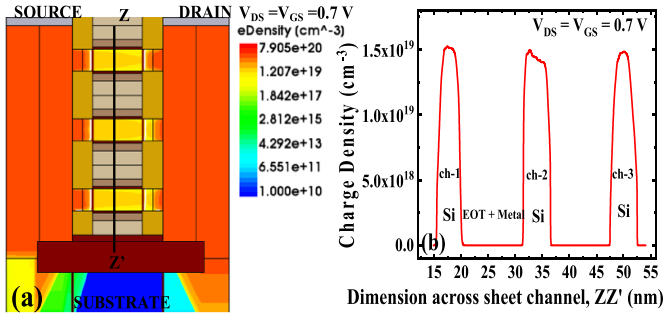

Figure 3. (a) Contour map of charge density distribution (b) line plot drawn at ZZ' for charge density of three-stacked vertically NS-FET.

3.1. Effect of device and carrier temperature

This sub-section deals with the coupled HD-TH transport model used to analyze the variation of device temperature (T_D) and carrier temperature (T_e). Figure 4 depicts the variation of device temperature (T_D) and carrier temperature (T_e) versus drain voltage at constant gate voltage ($V_{GS} = 0.7$ V). As shown in figure 4, while increasing the V_{DS}, the T_D and T_e are enhanced from 300 to 341 K and 350 to 2780 K, respectively. In linear regime (i.e. $V_{DS} < 0.2$ V), the low electric field keeps the value of T_D constant at approximately 300 K. However, in saturation regime (i.e. $V_{DS} > 0.2$ V), high electric field dominates and results in high joule heating and carrier heating. Due to this, charge carriers go into energy relaxation with enhanced optical phonon emission rates. Figures 5(a) and (b) shows the variation of spatial distribution for T_D and T_e and hot spot allocation near the edge of the channel-drain side.

$T_{D,\,max}$ is observed at the junction of the channel-drain region because hot carriers (highly energetic electrons) traveling towards the drain side undergo severe scattering with optical phonons at the interface of channel-drain. Hence, the

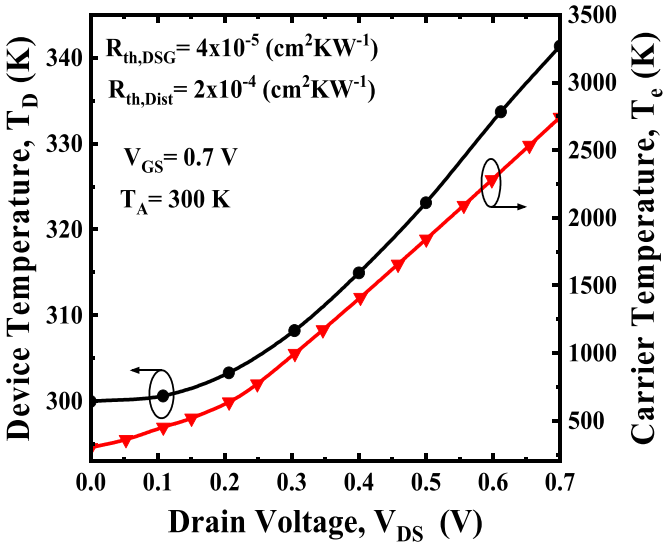

Figure 4. Variation of device temperature and carrier temperature with drain voltage at $T = 300$ K.

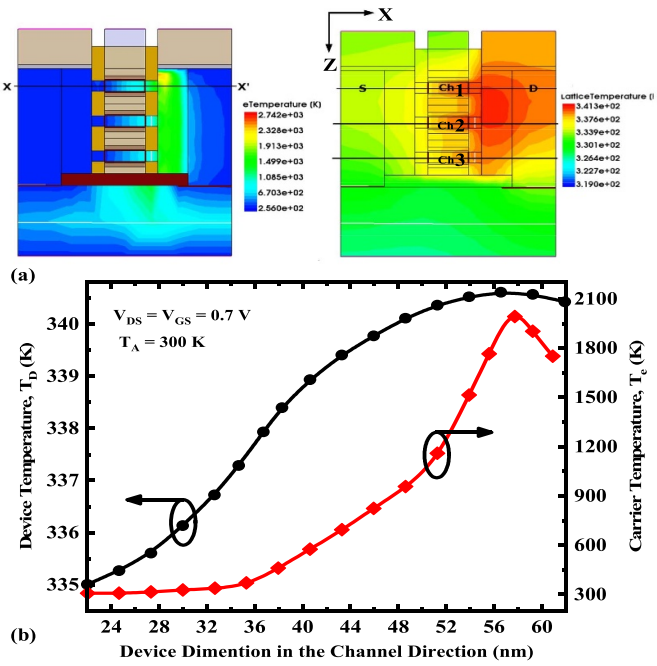

Figure 5. Variation of (a) contour plot of device temperature (T_D) and carrier temperature (T_e) (b) cut-line plot of three-stacked vertically NS-FET at $T_A = 300$ K for both T_D and T_e.

excess kinetic energy of charge carriers starts dissipating to the lattice (figure 5(b)). Due to this optical phonon interaction with the mobile carriers, the device temperature continuously increases along the channel directions.

3.2. Impact of thermal resistance on SHE

In this sub-section, we have studied the SHE on NS-FET caused by the electrode's interface thermal contact resistance ($R_{th,DSG}$). Figure 6 shows the equivalent thermal resistance circuit showing the channel resistance (R_{ch}), spreading resistance

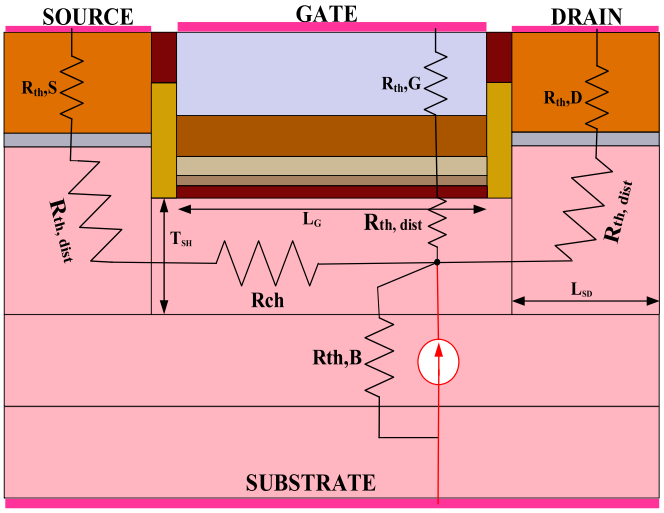

Figure 6. Equivalent thermal resistance circuit of for single channel of NS-FET device.

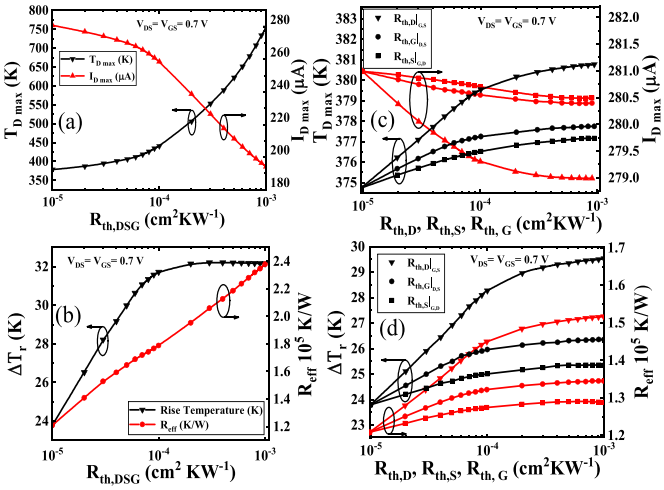

Figure 7. (a) Impact of interface thermal contact resistance on $T_{\mathrm{D\,max}}$ and $I_{\mathrm{D\,max}}$, (b) ΔT_{r} and R_{eff} with increasing interface thermal contact resistance ($R_{\mathrm{th,DSG}}$). (c) $T_{\mathrm{D\,max}}$ and $I_{\mathrm{D\,max}}$ and (d) ΔT_{r} and R_{eff} versus the effect of individual varying electrode's resistance ($R_{\mathrm{th,D}}$ or $R_{\mathrm{th,S}}$ or $R_{\mathrm{th,G}}$) while maintaining other electrodes at 1×10^{-5} cm^2 K W^{-1} and $T_{\mathrm{A}} = 350$ K, respectively.

(R_{sp}) as well as electrode's interface thermal resistance of the drain ($R_{\mathrm{th,D}}$), source ($R_{\mathrm{th,S}}$), gate ($R_{\mathrm{th,G}}$), and substrate ($R_{\mathrm{th,B}}$) [30]. Figure 7(a) shows the variation of maximum device temperature ($T_{\mathrm{D\,max}}$) from 378 K to 442 K (i.e. 16.9% increase) with change in interface thermal contact resistance ($R_{\mathrm{th,DSG}}$), increasing from 10^{-5} to 10^{-4} cm^2 K W^{-1} at a constant ambient temperature ($T_{\mathrm{A}} = 350$ K). Due to this, the saturation drain current ($I_{\mathrm{D\,max}}$) decreases from 280.8 to 258.18 μA (i.e. 8.05% decrease). Figure 7(c) shows the impact of interface thermal contact resistance of individual electrodes viz drain ($R_{\mathrm{th,D}}$), source ($R_{\mathrm{th,S}}$), and gate ($R_{\mathrm{th,G}}$) on $T_{\mathrm{D\,max}}$ and $I_{\mathrm{D\,max}}$ while keeping other electrode's interface thermal resistance constant at 1×10^{-5} cm^2 K W^{-1}. As the value of interface thermal resistance of either $R_{\mathrm{th,D}}$, $R_{\mathrm{th,S}}$, and $R_{\mathrm{th,G}}$ is varying from 10^{-5} to 10^{-4} cm^2 K W^{-1}, the change in device temperature (ΔT_{D}) for $R_{\mathrm{th,D}}$, $R_{\mathrm{th,S}}$, and $R_{\mathrm{th,G}}$ is observed as 4.814 K, 1.79 K, and 2.517 K respectively. Due to this, the device saturation drain current ($\Delta I_{\mathrm{D\,max}}$) decreases by 1.8, 0.48, and 0.51 for interface thermal resistance of drain, source, and the gate electrode, respectively. It is observed that the effect of $R_{\mathrm{th,D}}$ on the SHE is more than $R_{\mathrm{th,S,}}$ and $R_{\mathrm{th,G}}$. This is due to the major allocation of device temperature towards the drain side than gate and source (figure 5).

The effect of drain interface thermal contact resistance ($R_{\mathrm{th,D}}$) on ΔT_{r} and $R_{\mathrm{th,\,eff}}$ is found to be more pronounced compared to the gate and the source thermal contact resistance ($R_{\mathrm{th,G}}$, and $R_{\mathrm{th,S}}$) because of the close vicinity of maximum temperature to the drain which increases the SHE (figure 7(d)). Intuitively, the relative dominance of $R_{\mathrm{th,D}}$ in increasing device SHE will be more. Therefore, with a proper device engineering solution to reduce the device SHE is the reduction of thermal contact resistance at the interface of the $R_{\mathrm{th,D}}$ and for this, one needs to choose the appropriate metal electrode near the drain contact, which will mitigate the maximum temperature of the NS-FET. Figure 7(b) describes that as the value of interface thermal contact resistance $R_{\mathrm{th,DSG}}$ is increasing from 10^{-5} to 10^{-4} cm^2 K W^{-1}, the device rise temperature (ΔT_{r}) and effective thermal resistance (R_{eff}) is enhanced by 32.2% and 65%, respectively. As $R_{\mathrm{th,DSG}}$ further increases above 10^{-4} cm^2 KW^{-1} the more heat energy will dissipate towards the drain side which causes a small variation on ΔT_{r}. The R_{eff} has a dependency on total heat flux and can be calculated as follow:

$$R_{\mathrm{eff}} = \frac{\Delta T_{\mathrm{r}}}{\text{total heat}} \left(\mathrm{K\,W^{-1}}\right) \tag{4}$$

where, $\Delta T_r = T_{Dmax} - T_A$.

3.3. *Impact of ambient temperature on SHE*

SHE-induced thermal degradation is severely affected by the variations of within-chip ambient temperature. As the transistor density increases, the average within-chip temperature will increase, which will degrade both the I_{ON} and I_{OFF} of the transistor. A quantum corrected coupled HD and TD models are used to analyze the impact of ambient temperature SHE-induced thermal and electrical performance degradation of the NS-FET. It can be seen from figure 8(a), as the value of ambient temperature (T_{A}) is increasing from 300 K to 370 K, $T_{\mathrm{D\,max}}$ is increased from 341 K to 410 K (i.e. 20.23% increases), due to this the saturation drain current ($I_{\mathrm{D\,max}}$) decreases from 291 to 267 μA (i.e. 8.2% decrease) at $R_{\mathrm{th,DSG}} = 4 \times 10^{-5}$ m^2 K W^{-1}. This decrease in saturation drain current is apparent because the carrier mobility decreases as the temperature increases.

Figure 8(b) shows the effect of ambient temperature on effective thermal resistance (R_{eff}) and rise temperature (ΔT_{r}). At $T_{\mathrm{A}} = 300$ K, the value of R_{eff} and ΔT_{r} is 1.27×10^5 K W^{-1} and 23.7 K, respectively. The simplified SHE can also be captured without considering the lattice heat flow equation, as shown in figure 9. Due to this, $I_{\mathrm{D\,max}}$, and $T_{\mathrm{D\,max}}$ is increased

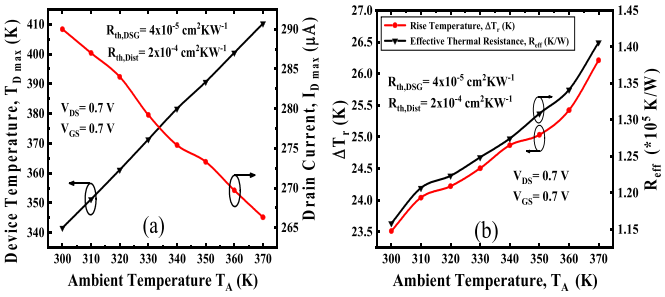

Figure 8. 7 Impact of ambient temperature variation on (a) device temperature $T_{\mathrm{D\,max}}$ and drive current ($I_{\mathrm{D\,max}}$) (b) rise temperature ΔT_{r} and effective thermal resistance R_{eff} of NS-FET.

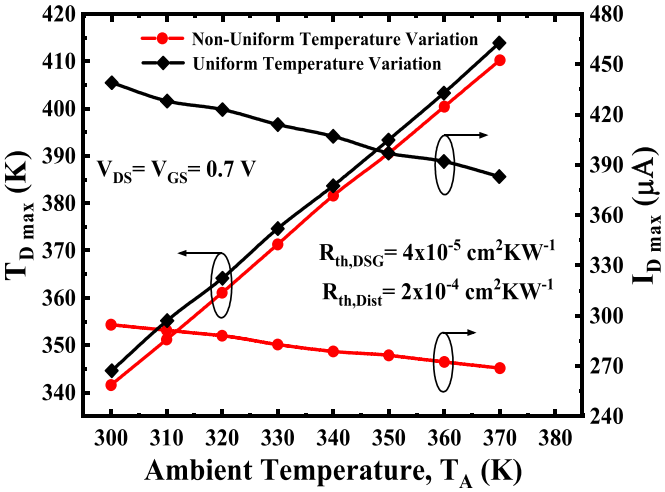

Figure 9. 8 Variation of maximum device temperature ($T_{\mathrm{D\,max}}$) and maximum drain current ($I_{\mathrm{D\,max}}$) versus ambient temperature considering uniform and non-uniform temperature.

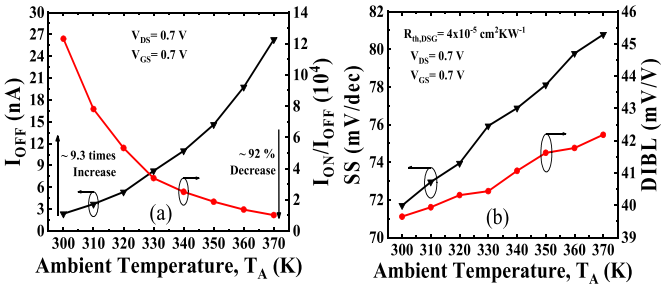

Figure 10. 9 Impact of ambient temperature variation on (a) leakage current (I_{OFF}) and driving current ratio ($I_{\mathrm{ON}}/I_{\mathrm{OFF}}$) (b) SS and (DIBL) of NS-FET.

by 49.5% and 1.15%, respectively. The ambient/sink temperature not only degrade the device temperature but also the device ON current (I_{ON}) and OFF current (I_{OFF}) as shown in figure 10(a), which elucidate the increase in I_{OFF} and decrease in $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio with increasing T_{A}. As the value of T_{A} is increasing from 300 K to 370 K the value of I_{OFF} is enhanced from 2.9 to 27 nA (increment by a factor of 9.3) which deteriorates the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ from 12×10^4 to 1×10^4 (91.6% degradation). Figure 10(b) shows the effect of T_{A} on DIBL and

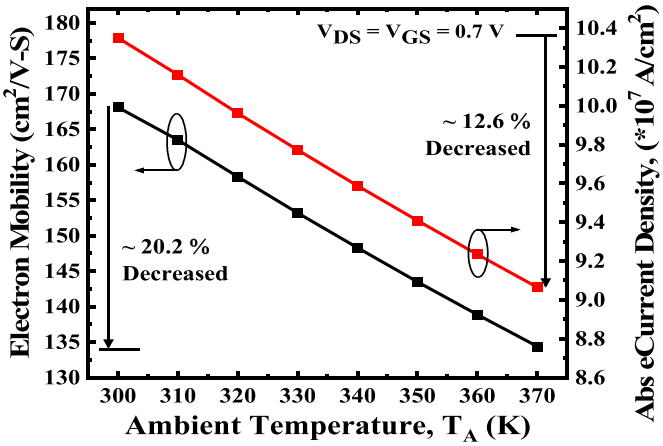

Figure 11. 10 Ambient temperature effect on electron mobility and absolute electron current density of NS-FET.

SS of the NS-FET. Due to the deleterious effect of ambient temperature-induced SHE, the DIBL is raised from 38.8 to 41.9 mV V^{-1} (i.e. 5.27% increase), and SS is increasing from 71.5 to 81.1 mV dec^{-1} (i.e. 13.4% increase). Increasing the value of T_{A} will result in high penetration of the Fermi tail into the conduction band energy, and this phenomenon will energies the charge carrier to cross the Fermi tail at the source-channel interface barrier. Due to this the leakage current (I_{OFF}) will increase, hence the value of SS increases. Figure 11 shows the decrease in carrier mobility from 168 to 134 cm^2 V^{-1} s^{-1} (i.e. 20.2% decrease) which results in degradation of electron current density from 1.035×10^7 to 0.905×10^7 A cm^{-2} (i.e. 12.6% decrease) as T_{A} is increased from 300 K to 370 K. As the ambient temperature increases, the optical phonon population increases, which will increase the carrier electron momentum, and due to the random scattering of the electrons, the mobility decrease. Figure 12 shows the variation of device temperature by increasing the ambient temperature from 300 K to 370 K with a step size of 10 K for the three-stacked NS-FET in the channel direction. With a uniform variation of T_{A}, the maximum gradient of device temperature is present in the channel region compared to the drain and source region. Moreover, the variation of the device temperature of the top channel is more pronounced compared to the bottom channel as the hot carriers moving towards the drain side undergo more scattering with phonon emission due to the enhanced charge density in the top channel. This results in higher joule heating and carrier heating. The bottom channel is less severely affected by this phenomenon due to the heat dissipation of the channel via the substrate. Further, in this manuscript, we have also compared the SHE-induced performance degradation of NS-FET with the conventional FinFET architectures. Table 2 shows the fair comparison between the thermal and electrical performance characteristics of NS-FET, bulk FinFET, and SOI-FinFET. The bulk and SOI FinFET devices are well-calibrated with the reported experimental data using TCAD simulation [39, 40]. After calibrating the bulk and SOI FinFET, the channel length and spacer length are tuned to the values taken for NS-FET to match the reported

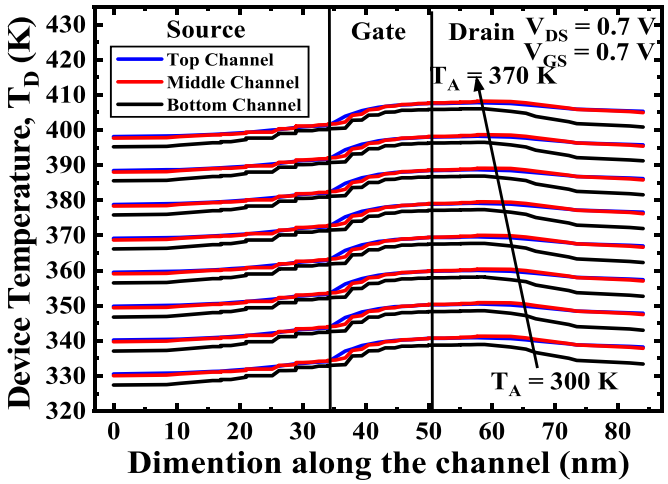

Figure 12. Variation of device temperature (T_D) along the channel direction of three-stacked vertically NS-FET.

Table 2. Impact of ambient temperature variation (when T_a is varying from 300 K to 370 K).

Parameter	NS-FET	Bulk-FinFET	SOI-FinFET
Device Temperature (K)	20.23%	17.8%	20.63%
Drain Current (A)	8.2%	6.1%	4.08%
I_{ON}/I_{OFF}	92%	88.24%	62.5%
SS (mV dec^{-1})	12.95%	23.71%	27.79%
DIBL (mV V^{-1})	11.8%	5.62%	3.32%

dimensions of the NS-FET for a fair comparison. We observe that, in NS-FET, the impact of SHE induced thermal degradation can potentially worsen the electrical characteristics compared to the FinFET as a low thermal conductivity material surrounds the channel regions of NS-FET.

4. Conclusion

In this paper, using well-calibrated TCAD simulations, we have investigated the SHE induced thermal degradation of stacked Nanosheet FET. Our simulation framework employed the quantum-corrected DD coupled hydrodynamic and thermodynamic models to get insight into the device temperature and carrier temperature profiles. The baseline NS-FET is well-calibrated with the experimental data using TCAD *Sentaurus*. The increase in ambient temperature from 300 K to 370 K increases the device temperature (increase by 20.23%, i.e. 341 K to 410 K), decreases the ON current (decrease by 8.2%, i.e. 291 μA to 267 μA), increases the OFF current by 9.3x, and reduces the I_{ON}/I_{OFF} by ∼91.6%. The increase in device temperature ($T_{D\,max}$) and reduction in I_{ON} current is also observed with a varying thermal resistance of the electrodes. In this manuscript, we have also compared the performance metrics of NS-FET with conventional FinFET and found that the NS-FET is more severe to the thermal degradation. Hence, the obtained results reveal that the ambient temperature and the interface thermal contact resistance strongly affect the device performance, which, in turn, degrades the electrical-thermal characteristics and reliability of the device.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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