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Investigation of Analog/RF and linearity performance with self-heating effect in nanosheet FET

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A R T I C L E I N F O

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A B S T R A C T

In vertically stacked gate-all-around Nanosheet FET (NSFET), the channels/sheets are wrapped by a low thermal conductivity material, which hinders the active heat flow path and, thus, raises reliability concerns. Therefore, the role of temperature, i.e., ambient condition and self-heating effect (SHE), become prime objectives that must be adequately addressed. In this work, through extensive TCAD simulations, we analyzed the DC/Analog/RF/Linearity characteristics of an NSFET, considering the cumulative effect of ambient temperature and SHE. Using well-calibrated TCAD models, we investigated: (i) the variation in device characteristics with and without considering SHE; (ii) the impact of SHE and ambient temperature on Analog/RF and Linearity characteristics using well-defined figure-of-merits (FoMs); (iii) the device optimization, i.e., the significance of the varying number of sheets (Nsheet) with considering SHE for optimal performance; (iv) the impact of varying temperature over the voltage gain of an NSFET-based common source (CS) amplifier considering SHE. The temperature variation (including SHE) significantly affects the ON current (e.g., reduced by 9.4%), resulting in the modulation in transconductance (g_m). Therefore, the designed CS amplifier's gain is also altered by temperature variation (e.g., ranging from 250 K to 400 K). Hence, the proposed analysis is worth exploring to acquire the design guidelines for optimal and reliable DC/Analog/RF/Linearity characteristics of a Nanosheet transistor under various temperature conditions.

1. Introduction

Affordable low-power and high-frequency devices continue in demand for wireless communication and next-generation applications [1,2]. In general, the higher transconductance (g_m) and lower output conductance (g_d) are required merits for high-frequency (95 GHz to 3 THz) and wireless communication (5G mm-wave) for high data transfer rate [3,4]. Over the numerous conventional devices such as FinFET, Tunnel FET, etc., the newly emerged vertically stacked gate-all-around Nanosheet FET (NSFET) attained much popularity owing to its higher driveability in the same footprint area as FinFETs. NSFETs provide increased leakage current control, better channel electrostatic control, lower output conductance (g_d), and less drain-induced barrier lowering (DIBL) compared to FinFET [5–7]. A wide variety of research is continuing to explore the significant impact of NSFET in DC/Analog/RF applications. Recently, it has been reported that the maximum

Oscillation frequency (f_{MAX}) and cutoff frequency (f_T) are higher in NSFET when compared to FinFET, which can be further enhanced by optimizing the device dimension [8–10]. Further, for the ability of the CMOS devices to operate in the gigahertz (GHz) range, a thorough analysis and optimization of the linearity characteristics are required. One can ensure a minimum value of intermodulation distortion and higher-order transconductance harmonics present at the output through some rigorous parameters, such as g_{m2}, g_{m3}, VIP_2, VIP_3, IMD_3, IIP_3, and 1-dB compression point (1-CP), which are quite efficient and less time-consuming approaches for defining the performance merits. Despite excellent characteristics, the Nanosheet FET suffers from a critical issue of self-heating effect (SHE) due to the confined intrinsic geometry of the channels/sheets surrounded by the low thermal conductivity material that hinders the heat flow path [11–15]. Our recent publications addressed a few of these issues for a reliable NSFET operation [16,17].

However, the complete analog and linearity analysis of the NSFET, considering the SHE is not yet explored and requires proper

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investigation. Therefore, in this paper, we investigated the analog/RF and linearity performance merits of NSFET considering the self-heating effect and compared the results with and without (w/o) SHE. Thus, analyzing the analog/RF and linearity performance parameters considering the SHE of any FET is pivotal to getting insight into the high-frequency RF application. ***The key contributions are*** (*i*) analysis of the impact of the SHE on device characteristics; (ii) investigation of temperature impact with and w/o SHE on various analog/RF parameters; (*iii*) study of linearity metrics of the NSFET considering the SHE; (i*v*) impact of ambient temperature on multi-sheet NSFET; (*v*) design and investigation of an NSFET based common source (CS) amplifier and impact of temperature on its functioning.

2. Device structure and simulation setup

A *3D* schematic and cross-section view of NSFET is shown in Fig. 1. The channels/sheets are stacked vertically between the source/drain (S/D) pads. Uniform doping is employed in.

S/D pads and in the channel region, whereas to emulate the S/D extension regions, Gaussian doping with a fixed decay tail is employed. The gate oxide stack comprises conventional SiO_2 and HfO_2, resulting in an effective oxide thickness (EOT) of 0.9 nm. The spacer Si_3N_4 over the extension regions is placed to suppress the effect of gate S/D capacitances [18]. The effective width $\{W_{eff} = 2(t_w + t_{ch})N_{stack}N_{sheet}\}$ is a function of the number of sheets (N_{sheet}) and the stacks (N_{stack}). We employed the *Sentaurus* TCAD tool [19] in our analysis. The drift-diffusion (DD) model is included in the simulation setup for considering carrier transport coupled with the density gradient model to capture the channel's spatial and electrostatic quantum confinement. The modified local density approximation model (MLDA) is incorporated to consider the carrier distribution near the oxide/silicon interface. Further, the vertical field Mobility, ballistic mobility, and high field saturation model are used to render the short channel effects (SCEs). The inversion and accumulation layer (IAL) mobility model accounts for degradation due to Coulomb scattering, surface roughness scattering, and phonon scattering on mobility [16]. The Shockley-Read-Hall (SRH) and Auger models consider the generation and recombination of the charge carriers. The Slotboom model captures the doping/temperature-dependent bandgap narrowing effect. The models are well-tuned to match the simulation data with the experimental data [5], as shown in Fig. 2. All the device parameters used in the simulation are mentioned in Table-1 unless stated otherwise. Generally, the interface between the metal and semiconductor in the source/drain-metal (M_0) region significantly impacted the device's electrical and thermal performance. This is primarily due to the formation of a Schottky barrier caused by Fermi-level pinning, leading to increased contact resistances at the source and drain, affecting the drain current. However, to address this issue and enhance the performance of sub-5 nm nanoscale devices, a self-aligned silicidation process, also known as salicidation is employed. This process effectively reduces the contact resistances, resulting in improved electrical performance. Therefore, our analysis considered S/D metal interface distributive contact resistance of 8.4×10^{-10} Ωcm^2 [16,20]. In general, the thermal conductivity of NSFET is a function of thickness, temperature, and phonon-dopant impurity mass fluctuation scattering. Thus, as mentioned in our previous publication, we considered the Boltzmann transport equation for phonons with relaxation time approximation-based thermal conductivity (k_{th}) [16]. Further, the quantum-corrected DD model coupled with hydrodynamic and thermodynamic models is included to capture the SHE-induced thermal degradation [19]. Fig. 3 shows the electron density and electron mobility profile of the NSFET. At higher drain voltage ($V_{DS} = 0.7$ V), the peak inversion charge density is shifted towards the oxide-channel interface due to the confinement of the electrostatic field near the interface (Fig. 3a). The electron densities vary in the NSFET based on the sheet located in the stack and also with sheet thickness. The peak inversion electron density is higher in the top channel (Ch-1) than in the bottom (Ch-3) due to less series resistance at the S/D contact. The electron mobility decreases with an increase in electron density (Fig. 3b).

3. Results and discussion

This paper explored the DC/Analog/RF/Linearity performance merits of an NSFET, considering the self-heating effects in an account. Moreover, the impact of ambient temperature and SHE is investigated in an NSFET-based common source amplifier design. The section is subdivided as.

3.1. DC performance metrics influenced by SHE

Fig. 4 shows the spatial distribution of the lattice temperature (T_L) profile and its impact on the electrical transfer characteristics. Due to the accumulation of heat in the channel region, the maximum temperature (hotspot) in the NSFET increases from 300 K to 393.2 K (Fig. 4a), which results in drain current (I_{DS}) degradation by ~6.65% (Fig. 4b). The bottom sheet (Ch-1) has observed a lower temperature due to the heat sink through the substrate (Fig. 4c). However, the top sheet (towards the drain side) got maximum hotspot owing to the accumulation of more charges, causing more scattering. Temperature dependence is a severe issue in thin and short-channel devices as it affects carrier mobility. Fig. 5 shows the impact of the SHE on DC electrical characteristics by varying the ambient temperature (i.e., CPU/IC chip temperature) from 250 K to 400 K. In general, the impact of varying the ambient temperature can be captured by the change in the energy gap and mobility of

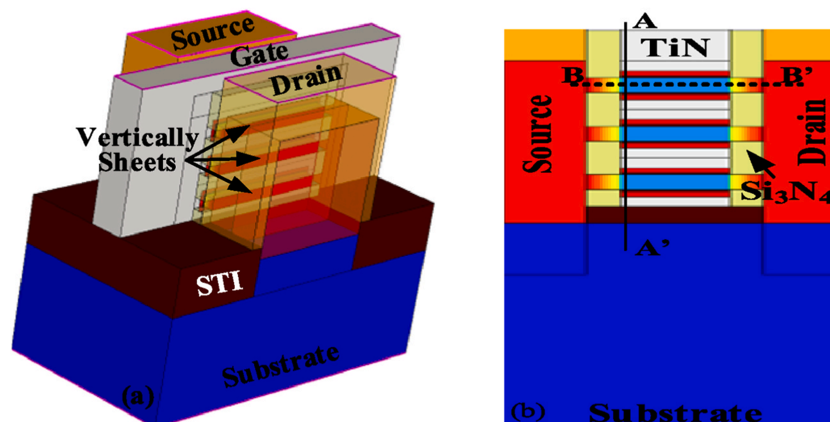

Fig. 1. (a) *3D* isometric schematic of a three-stacked Nanosheet FET; (b) cross-section view showing the different regions/sections/cutlines of the NSFET.

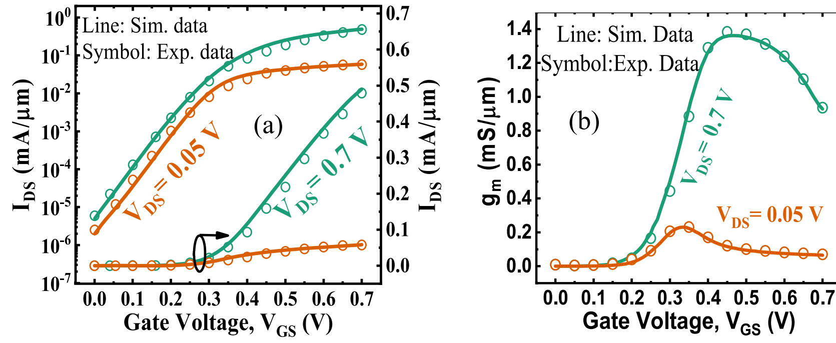

Fig. 2. Calibration of the TCAD models against the experimental data [5] (a) transfer characteristics (I_{DS}-V_{GS}); (b) transconductance (g_m) characteristics.

Table 1
Parameter table.

Parameters	Value	Parameters	Value
Gate Length (L_g)	12 nm	SiO_2 (IL) thickness	0.6 nm
Channel Width (t_w)	25 nm	Substrate doping (N_S)	10^{18} cm^{-3}
Channel thickness (t_{ch})	5 nm	Channel Doping (N_c)	10^{16} cm^{-3}
Si_3N_4 spacer Permittivity	7.9ϵ_o	S/D doping ($N_{S/D}$)	10^{21} cm^{-3}
HfO_2 Permittivity	22ϵ_o	Interfacial EOT	0.9 nm
HfO_2 thickness	1.7 nm	Spacer Length (L_{SP})	5 nm
Thermal Conductivity ($WK^{-1}cm^{-1}$)			
HfO_2Thermal Conductivity	0.023	Gate Metal Conductivity	0.192
SiO_2 Thermal Conductivity ($Ksio_2$)	0.014	S/D Metal (M_0) Thermal Conductivity ($K_{S/D,M}$)	1.7

the charge carriers, given as [21]:

$$E_g(T) = E_g(0) - \frac{\alpha T_0^2}{T_0 + b}\ ; \quad \mu_{eff} = \mu_{eff0}\left(\frac{T_L}{T_0}\right)^{-2} \tag{1}$$

where $\alpha = 4.73\times10^{-4}$ eV/K, $b = 636$ K, and $E_g(0) = 1.21$eV for silicon. T_0 is the room temperature (i.e., 300 K), and T_L is the lattice temperature. μ_{eff} and μ_{eff0} are the effective mobility obtained at lattice and room temperature, respectively. Eq. (1) shows that the energy gap and mobility decrease as the ambient temperature increases. At higher gate voltage (V_{GS}), the strong inversion occurs below the gate oxide region. When the ambient temperature increases, the charge carrier scattering dominates over the bandgap reduction, which reduces the carrier mobility and, thus, the drain current (I_{DS}). Further, due to SHE, the non-equilibrium lattice temperature in the channel region causes mobility degradation, causing I_{DS} degradation, as shown in Fig. 5a-b. On the contrary, the I_{OFF} increases with the increase in temperature (Fig. 5c) because the Fermi tail penetrates to higher conduction band energy levels, which enables the energetic carriers to cross the source-channel barrier [12]. As T_A increase from 250 K to 400 K, the SS increases by ~60%, and V_{th} reduces by ~35%. The calculated dV_{th}/dT is −0.5546 mV/K (Fig. 5d). However, considering SHE, the I_{OFF} and SS do not show significant variation due to weaker scattering phenomena.

3.2. Analog/RF metrics considering SHE

This sub-section analyzes the impact of temperature on the analog/RF performance of the NSFET with and without considering SHE. The important analog/RF parameters, such as transconductance (g_m), gate capacitance (C_{gg}), gain-bandwidth product (GBP), unity gain cutoff frequency (f_T), and transconductance frequency product (TFP), have been thoroughly investigated. In general, g_m is a function of (V_{GS}-V_{th}), (W/L), C_{ox}, etc. [22]. Thus, indirectly, g_m is a function of temperature also, as temperature modulates the V_{th} of the device. The present work only analyzes the impact of V_{GS} and temperature on g_m, keeping all the parameters constant.

As temperature rises, the effective energy gap decreases, and the intrinsic carrier concentration increases in the channel, causing a diffusion phenomenon that increases the g_m at lower V_{GS} (Fig. 6a). When V_{GS} increases above a certain value, NSFET indicates strongly inverted channels. In this case, the conduction current is primarily due to drift, and both mobility and electric field influence the temperature dependence of the g_m (Fig. 6a). With a further increase in V_{GS}, the surface potential gets pinned. Further, due to the self-heating effect at higher gate voltage, the non-equilibrium lattice temperature (T_L) causes severe mobility degradation resulting in g_m degradation. With the rise in T_A, more scattering occurs and decreases in mobility, further reducing g_m. Thus, the inversion charge density does not profoundly modulate with V_{GS}, i.e., $\partial I_D/\partial V_{GS}$ decreases as the drain current gets saturated. The zero-temperature-coefficient (ZTC), as shown in Fig. 6a, is where the temperature has a negligible impact on devices. Fig. 6(b–c) shows the total gate capacitance (C_{gg}) and gate-to-drain capacitance (C_{gd}) with and

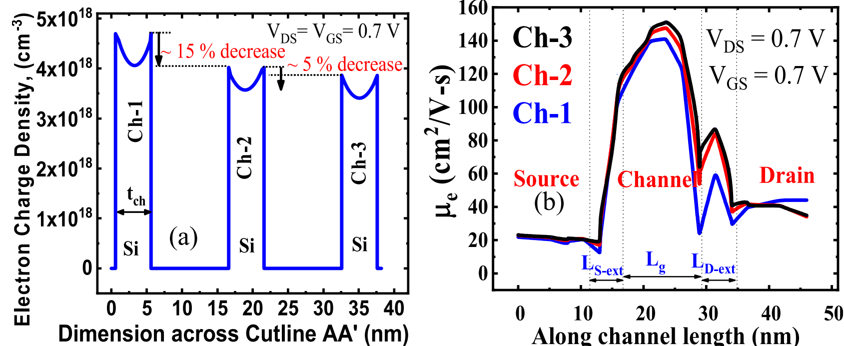

Fig. 3. (a) the electron density across the cutline AA'; (b) electron mobility (μ_e) along the channel length in each sheet.

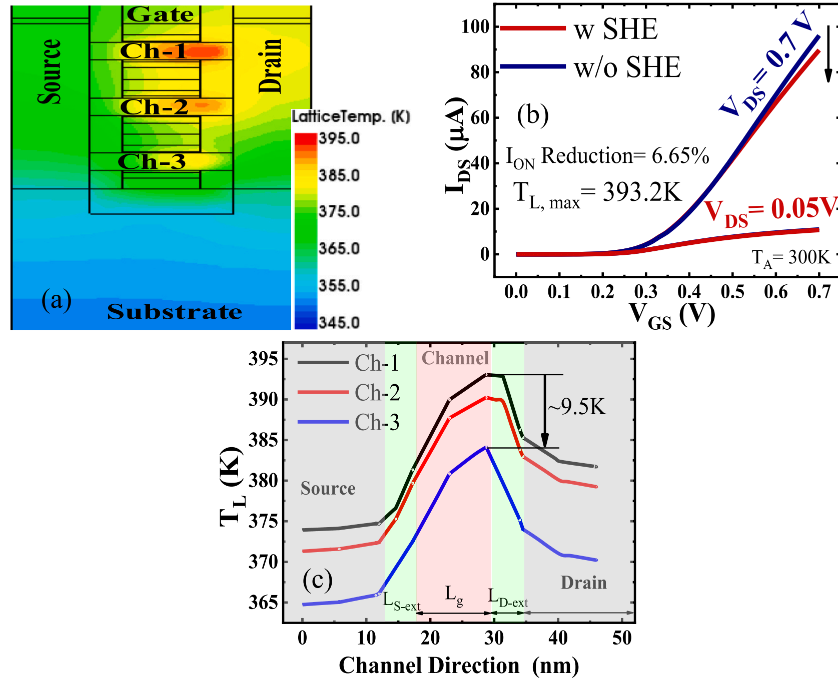

Fig. 4. Shows (a) a contour plot of the asymmetric spatial distribution of the lattice temperature (T_L) profile; (b) I_{DS}-V_{GS} characteristics with and w/o considering SHE; (c) T_L profile along the channel direction at V_{GS}=V_{DS}= 0.7 V..

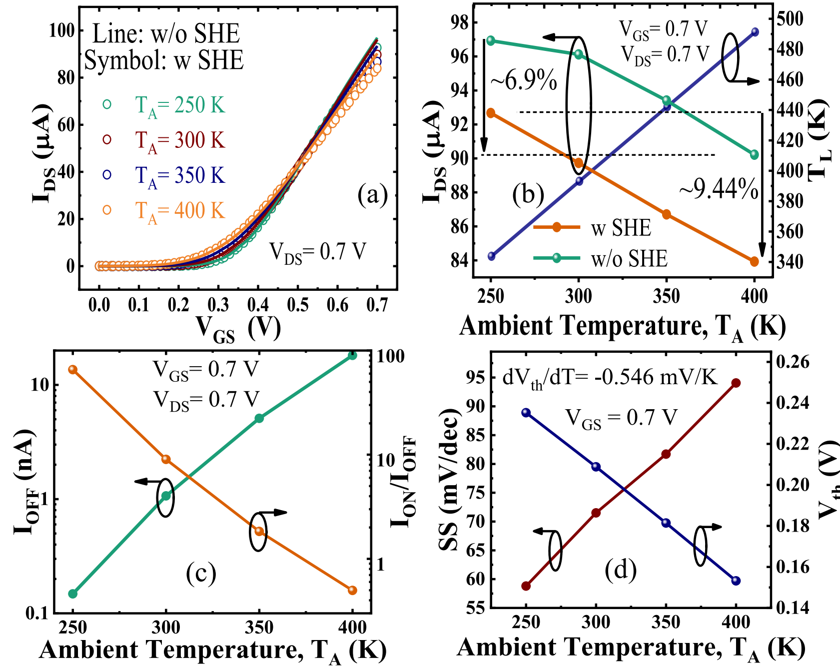

Fig. 5. Shows the impact of temperature on (a) I_{DS}-V_{GS}; (b) percentage degradation in I_{DS} and influence on T_L; (c) OFF current (I_{OFF}) and switching ratio (I_{ON}/I_{OFF}); (d) subthreshold swing (SS) and threshold voltage (V_{th})..

without SHE with varying temperatures. Owing to SHE, the scattering of the carrier at the drain extension increases; therefore, a higher lateral field is needed to achieve the same ON current (measured at V_{GS}=V_{DS}=0.7 V). Hence, the C_{gd} decreases with the inclusion of SHE, as shown in Fig. 6c. In addition, the SHE increases the lattice temperature, extending the carrier Fermi tail at the source-channel junction. Therefore, the gate-to-source capacitance (C_{gs}) would increase, resulting in an increase in C_{gg} (as the total gate capacitance is the combination of C_{gd} & C_{gs}), as shown in Fig. 6b.

In general, a transistor's unity gain cutoff frequency (f_T) is defined at the frequency when short circuit current gain becomes unity [23]. Thus, f_T is calculated as:

$$f_T = \frac{g_m}{2\pi \, x \, C_{gg}} \tag{2}$$

where C_{gg} is the sum of gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}). These capacitances have been extracted using the small-signal AC analysis in mixed-mode simulation at 1 MHz

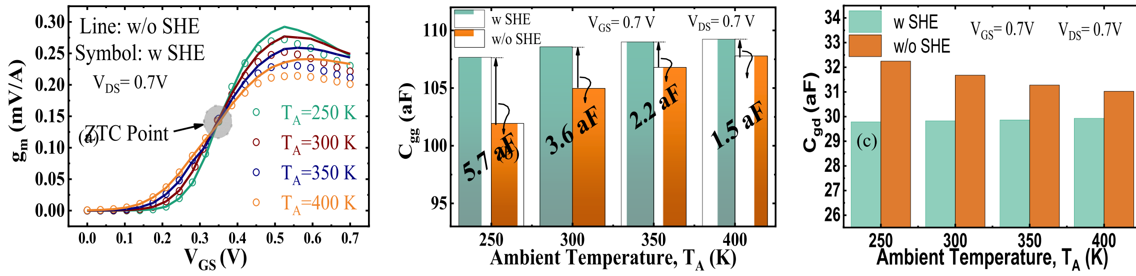

Fig. 6. Impact of temperature on (a) transconductance (g_m); (b) gate capacitance (C_{gg}), and (c) gate-to-drain capacitance (C_{gd}).

frequency [24]. Eq. (2) shows that f_T depends on g_m and C_{gg}. In turn, f_T has temperature dependence (Fig. 7a), which shows that the peak of the f_T decreases with an increase in temperature due to the decrease in g_m (Fig. 6a). Due to SHE, the temperature increases; therefore, the reduction in maximum f_T is due to the dominance of g_m as compared to C_{gg} [Fig. 7a (inset)]. The percentage change in cutoff frequency (f_T) is calculated as:

$$\%f_{T,max}\ Reduction = \frac{f_{T,w/oSHE} - f_{T\ w\ SHE}}{f_{T,w/o\ SHE}}$$

Therefore, the RF performance of the NSFET deteriorates with an increase in temperature. In addition, the GBP and TFP are also crucial parameters that require proper attention. The GBP and TFP can be described as [23,24]:

$$GBP = \frac{g_m}{2\pi x\ 10\ x\ C_{gd}};\quad TFP = \left(\frac{g_m}{I_{DS}}\right) x\, f_T \tag{3}$$

The GBP of the NSFET decreases due to a decrease in g_m with an increase in temperature (Fig. 7b). With consideration of SHE, a further reduction in GBP is observed as SHE affects the g_m. Further, a tradeoff between bandwidth and power could be obtained by TFP (Eq. (3)), which is also influenced by temperature (Fig. 7c). As the g_m and f_T decrease with the temperature, TFP follows the trend. In the subthreshold region, TFP linearly increases with V_{GS}, holds an optimal value at certain $V_{GS,}$ and decreases, further showing a decrement with SHE. Thus, a thorough investigation of the analog/RF performance merits with the self-heating effect of the NSFET revealed that the ambient temperature plays a significant role in performance merit optimization.

3.3. Linearity analysis considering SHE

The linearity characteristics should be analyzed and maintained for better analog/RF performance, which can be obtained by minimizing the distortion and signal-to-noise ratio.

The linearity of any system could easily be analyzed by relevant device parameters, such as second and third-order voltage intercept points (VIP_2 and VIP_3), third-order input current intercept points (IIP_3), third-order intermodulation distortion (IMD_3), and higher derivatives of g_m, i.e., $g_{m,n} = 1/n!\partial^n I_{DS}/\partial V_{GS}{}^n$ for n = 2,3, etc. These parameters can be defined as [25]:

$$VIP_2 = 4\ x \left(\frac{g_{m1}}{g_{m2}}\right);\quad VIP_3 = \sqrt{24\ x \left(\frac{g_{m1}}{g_{m3}}\right)} \tag{4}$$

$$IIP_3 = \frac{2}{3}\ x \left(\frac{g_{m1}}{g_{m3}\ x\ R_s}\right) \tag{5}$$

$$IMD_3 = \left[\frac{9}{2}\ x\ (VIP_3)^3\ x\ gm_3\right]^2 x\ R_s \tag{6}$$

$$1 - CP = 0.22\ x\ \sqrt{\frac{g_{m1}}{g_{m2}}} \tag{7}$$

The second and third-order harmonics cause significant distortion/noise in the transistor, enhancing the disturbances in FET-based communication systems. Fig. 8 shows the impact of varying temperatures on g_{m2} and g_{m3} of NSFET with and w/o consideration of SHE. The g_{m2} and g_{m3} decrease while increasing the temperature, which shows the improved linear performance of the NSFET, which further decreases with SHE. Therefore, the temperature impact with SHE on g_{m2} and g_{m3} mitigates the disturbances in the communication system. For higher V_{GS}, the value of g_{m2} becomes negative due to the lowering of g_m (Fig. 6a). The voltage V_{GS} at which g_{m2} becomes zero will give the singularity in g_{m3}, which will determine the DC bias point for the optimum operation of the NSFET. Further, VIP_2, VIP_3, and IIP_3 are other essential parameters to examine the linearity of NSFET, and for better linearity, VIP_2, VIP_3, and IIP_3 should be maximum. VIP_2 and VIP_3 represent the extrapolated input voltage, for which the first-order harmonic equals second-order and third-order harmonics, respectively. The effect of temperature variation on VIP_2 and VIP_3 of NSFET is shown in Fig. 9. It can be depicted that the peak value of VIP_2 and VIP_3 increases with an increase in temperature, which perceives the improved linearity characteristics. The same trend is observed with consideration of the SHE. IIP_3 relates to the extrapolated input current where first and third-order harmonic currents are equal. The IMD_3 describes the intermodulation current where first and third-order harmonic currents are equal and should be minimum for better linearity. Here R_S = 50 Ω (in Eq. (6)) is generally considered for most RF applications [22]. Fig. 10 shows the temperature impact on IIP_3 and IMD_3 for varying V_{GS}.

It is clear that the peak value of IIP_3 is enhanced with the rise in

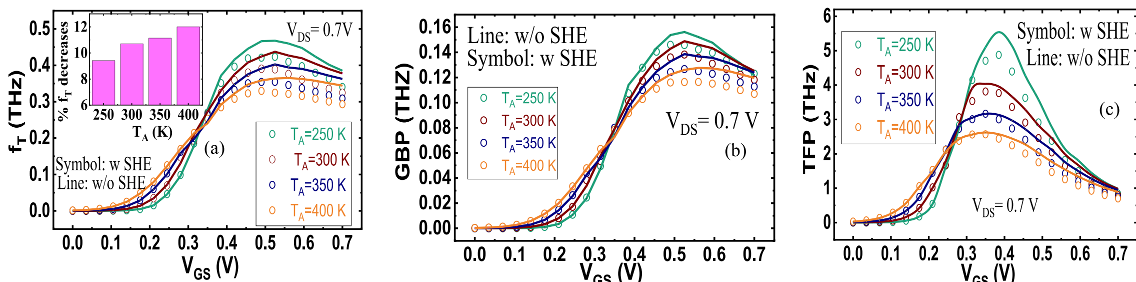

Fig. 7. Impact of ambient temperature on (a) unity gain cutoff frequency (f_T); (b) gain bandwidth product (GBP); (c) transconductance frequency product (TFP).

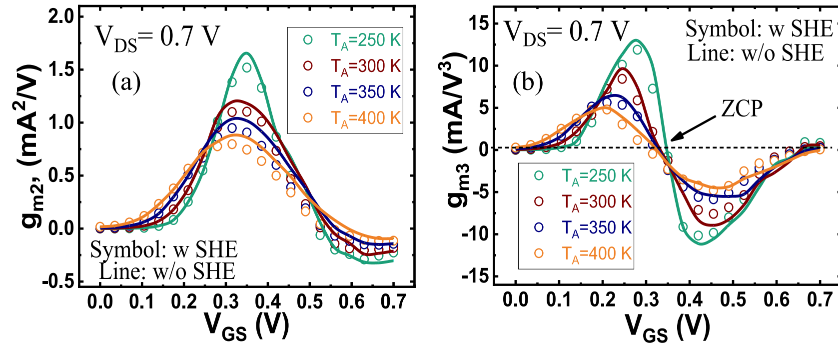

Fig. 8. Impact of temperature on higher-order transconductance (a) g_{m2} and (b) g_{m3} of the NSFET.

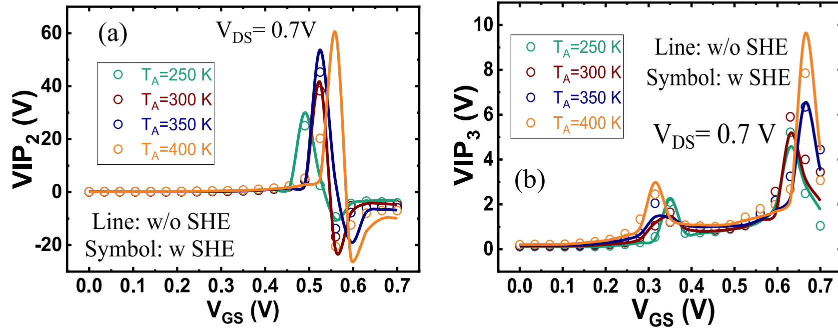

Fig. 9. Impact of temperature on voltage intercept points (a) VIP_2 (b) VIP_3 of the NSFET with applied V_{GS}.

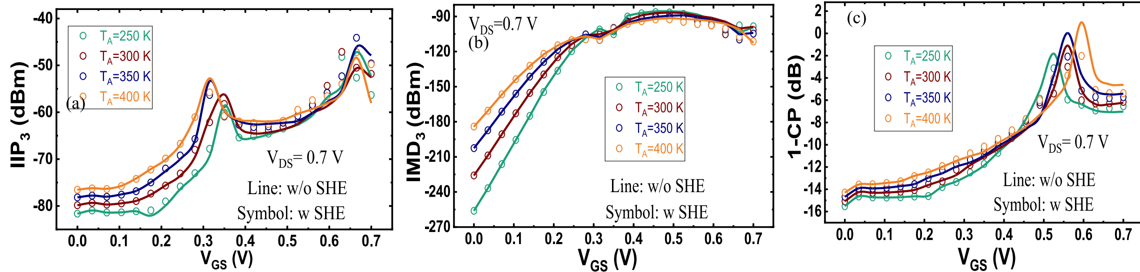

Fig. 10. Impact of temperature on (a) third-order input current intercept points (IIP_3); (b) third-order intermodulation distortion (IMD_3); (c) 1-dB compression point with applied V_{GS} in NSFET.

temperature for the weak to moderate inversion region, which expresses enhanced linearity performance. With considering SHE, the IIP3 (Fig. 10a) improves as temperature increases. IMD_3 arises due to nonlinear static characteristics exhibited by the NSFET, which can cause signal degeneracy. The IMD_3 decreases as temperature increases (Fig. 10b) for moderate to strong inversion regions, reducing the distortion. It is discerned that IIP_3 is higher than IMD_3 due to the suppression of the hot carriers at the channel-dielectric interface. 1-dB compression point (1-CP) [Eq. (7)] describes the efficacy of linearity for the NSFET. It signifies the level of small-signal input current from (Fig. 10c). A higher value of 1-CP is obtained for the moderate which the device's gain drops by '1 dB'. The 1-CP of the NSFET steadily rises with the increase in temperature to strong inversion region. Thus, *all in all*, the linearity performance metrics of the NSFET get improved as temperature increased.

3.4. Device (number of sheets) optimization considering SHE

Throughout this work, we analyzed the device behaviour with considering SHE, which is crucially dependent on the number of sheets (N_{sheet}). Increasing N_{sheet} would modulate the heat sink path (hotspot) and thus alters the characteristics. Fig. 11 shows that the increase in N_{sheet} improves the current drivability as the overall device area would increase. However, the temperature adversely impacted the I_{DS} and it is reduced by ~2.64 μA for a single nanosheet (SH-1) with a temperature increase (Fig. 11a). It is noteworthy that the current does not reduce linearly with a rise in temperature for a higher N_{sheet} because, with an increase in N_{sheet}, the charges increase at the drain side, causing more scattering.

Thus, considering SHE with varying temperatures does not significantly impact the I_{DS} and g_m degradation (Fig. 11b). Fig. 11 (c) shows that as N_{sheet} increases, the effective width increases, which increases the channel charge; thus, capacitance increases. For larger N_{sheet} with considering SHE, the hotspot temperature ($T_{L,max}$) increases, which modulates the effective bandgap and increases the channel charge; thus, capacitance would be higher than at the lower sheets.

3.5. Analog circuit aspect considering SHE

As in previous subsections, we have seen that SHE plays a crucial role in modulating the device characteristics. The significance of SHE with the varying ambient temperature is now articulated in a vertically three-

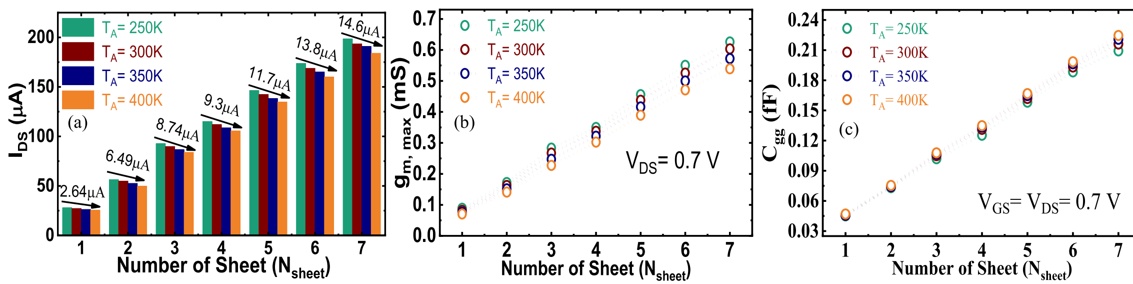

Fig. 11. Shows the impact of temperature and varying number of sheets (N_{sheet}) on (a) drain current (I_{DS}), (b) maximum transconductance ($g_{m, max}$), and (c) total gate capacitance (C_{gg}) with considering SHE..

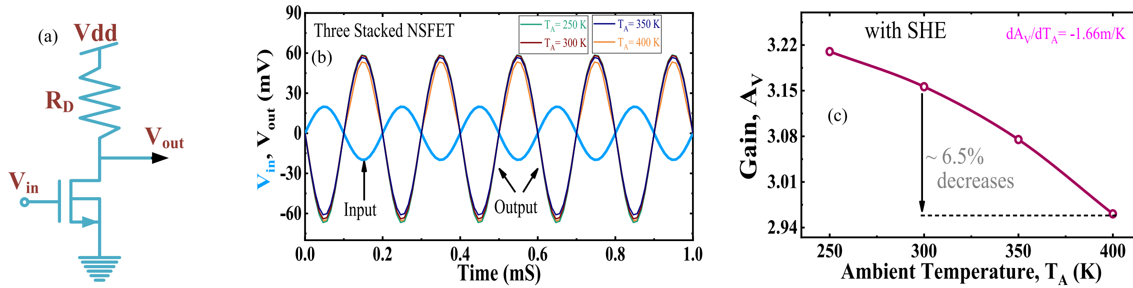

Fig. 12. Shows (a) Vertically three-stacked NSFET-based single-stage resistive load common source (CS) amplifier; (b) the input-output waveform for varying temperatures from 250 K to 400 K; (c) the voltage gain decreases as ambient temperature increases..

stacked NSFET-based analog circuit. In this study, we opted for a single-stage common source (CS) resistive load amplifier and investigated the impact of temperature considering SHE, as shown in Fig. 12(a–b). A constant resistance R_D is considered, and the temperature coefficient of resistance (TCR) is not considered in the simulation to solely analyze the impact of SHE. A two-level Newton-Rapson coupled algorithm is invoked to solve the interdependence device and circuit co-simulation matrices [16]. The TCAD mixed-mode simulation is used to simulate the AC characteristics of the CS amplifier. The voltage gain (A_V) of an n-type NSFET-based amplifier is given as [10]:

$$A_V = V_{out}/V_{in} = -g_m \times (r_o // R_D) = -g_m R_D \tag{8}$$

where r_0 and RD are the output and load resistance, respectively.

At the quiescent point (Q-point), the r_o is very large (i.e., $r_o \simeq \infty$), which shows that the variation in the output voltage (V_{out}) is significantly dominated by the transconductance (g_m), and the gain is severely affected by self-heating with varying temperature. The Q-point of the baseline NSFET is selected based on the superposition of the load line and I_{DS}-V_{DS} characteristics. Fig. 12 (c) shows the voltage gain variation with temperature considering SHE. The A_V is reduced from 3.15 to 2.95 (i.e., ~6.5%) while the ambient temperature rises from 300 K to 400 K as the A_V is a vital function of g_m, which varies with temperature. Thus, a thorough investigation of NSFET considering SHE and varying ambient temperature has been proposed using device circuit co-design.

4. Conclusion

The crux of the paper is to explore the role of temperature with its intrinsic component, i.e., self-heating effect (SHE) and the extrinsic part (i.e., ambient temperature) on the DC/Analog/RF and Linearity characteristics of a Nanosheet transistor. Using well-calibrated TCAD models, we investigated the impact of ambient temperature on device characteristics and found that the increase in temperature degrades the electrical characteristics of the NSFET due to bandgap narrowing and carrier mobility degradation. With considering SHE, the analog/RF performance has been investigated using well-defined parameters such as g_m, C_{gg}, f_T, GBP, and TFP, which are deteriorated with the increase in temperature. However, the linearity performance merits such as g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3, IMD_3, and 1-CP of NSFET improved with increasing temperature. Further, we analyzed the impact of increasing temperature on the varying number of sheets (N_{sheet}) in NSFET. The temperature effect is more pronounced at a higher N_{sheet} value because the S/D pad area has limited conduction. Thus, detailed insight into SHE on NSFET with varying ambient temperatures provides a design guideline to fix the DC/Analog/RF/Linearity performance up to the mark.

Author statement

Sunil Rathore: Conceptualization, Methodology, Data curation, Software, Writing – original draft, Investigation, Rajeewa Kumar Jaisawal: Conceptualization, Methodology, Investigation, Software, P. N. Kondekar: Supervision, Visualization, Navjeet Bagga: Supervision, Writing- Reviewing and Editing, Corresponding Author, Conceptualization, Visualization

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper

Data availability

The authors do not have permission to share data.

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