# Design Optimization of Three-Stacked Nanosheet FET From Self-Heating Effects Perspective

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***Abstract*—Self-heating effect (SHE) is a severe issue arising in the nanoscale field-effect transistors (FETs). It raises the device's lattice temperature several degrees higher than the ambient temperature and degrades the driving current. The diamond-based dielectric material may be a promising candidate to mitigate the SHE due to its significantly larger thermal conductivity value ($k_{th}$ = 2000 $W.m^{-1}.K^{-1}$) than $SiO_2$ ($k_{th}$ = 1.4 $W.m^{-1}.K^{-1}$). In this paper, we have investigated the potential of crystalline diamond to mitigate the SHE-induced degradation in a partially depleted silicon-on-diamond Nanosheet FET (PDSOD NSFET). The results are compared with the partially depleted silicon-on-insulator (PDSOI) NSFET. Using extensive TCAD simulations, we investigated the impact of varying the ambient temperature and nanosheet thickness on the performance metrics of PDSOD and PDSOI NSFET. Thus, our analysis reveals that PDSOD NSFET is a viable alternative to alleviate the SHE-induced thermal degradation for the same footprint area of $SiO_2$ used in PDSOI NSFET.**

***Index Terms*—Silicon-on-insulator (SOI), diamond-like carbon (DLC), silicon-on-diamond (SOD), nanosheet, self-heating effect.**

## I. INTRODUCTION

INEVITABLE scaling of CMOS devices requires continued research on the emerging trends of semiconductor devices. In the last few decades, numerous non-planar devices have been proposed to achieve higher gate electrostatic control, which subsides the short-channel effects (SCEs) [1]–[3]. The gate-all-around (GAA) nanosheet transistors are among the alternatives gaining popularity owing to the high ON current in the same footprint area as conventional FinFET; therefore, paving the path for aggressive scaling below the 5nm node [4]–[7]. In general, the silicon-on-insulator (SOI) architecture possesses many advantages such as reduced sub-channel leakage current, power performance improvement, low parasitic capacitance, increased frequency, and immunity to process variation [8]–[10] compared to the bulk devices. Further, to avoid the constraints on threshold voltage and its sensitivity, the partially depleted SOI (PDSOI) is preferred over the fully-depleted SOI (FDSOI). The self-heating effects (SHE) become more pronounced in all such devices with the incessant scaling of the gate length and other device dimensions. Many methods have been reported to mitigate the SHE-induced degradation, such as quasi-SOI technologies [11], diminishing the buried oxide (BOX) thickness in SOI devices [12], and depositing the high thermal conductivity nitrite material instead of $SiO_2$ [13]. However, all such methods cannot be implemented easily in nanoscale GAA FETs due to the enhanced electric field in thin-film SOI [14]. Generally, the SOI device consists of a thin film of buried oxide ($SiO_2$) for electrical isolation of the bulk substrate. However, due to the low thermal conductivity of $SiO_2$ ($k_{th}$ = 1.4 $Wm^{-1}K^{-1}$), the heat dissipation path between the device's active region and bulk substrate ceases [15]. Consequently, the lattice temperature of the SOI-based devices enhanced significantly compared to bulk devices, resulting in reduced carrier mobility, subside transconductance, and device speed. SHE-induced degradation can be minimized by replacing the buried $SiO_2$ layer with a high thermal conductivity material, such as crystalline diamond, which has thermal conductivity (2,000 W $m^{-1}K^{-1}$), ∼1000 times higher than $SiO_2$ [16]. Due to its intrinsic properties, the crystalline diamond possesses excellent heat removal properties; thus, the SHE-induced thermal degradation can be mollified using SOD instead of the SOI layer. The fabrication feasibility offers a very smooth realizable interface between Si/diamond using the high-resolution transmission electron micrograph [17], which is compatible with the current integrated-circuit fabrication [18]. Further, using the different bonding techniques, the remote roughness scattering can be minimized [19]. Therefore, replacing the $SiO_2$ with the crystalline diamond can reduce the SHE and its induced thermal degradation in state-of-the-art nanoscale electronic devices.

This paper explored the potential of realizing the SOD layer in a three-stacked nanosheet transistor, an emerging device in which SHE plays a crucial role. Using well-calibrated TCAD models, we thoroughly investigate the electrical characteristics of the PDSOI and PDSOD NSFET. We have analyzed the impact of SHE-induced thermal degradation and varying the channel thickness ($T_{ch}$) on device lattice temperature ($T_L$), ON current ($I_{ON}$), and effective thermal resistance ($R_{eff}$) of the NSFET. The rest of the paper is organized as follows: Section II explains the PDSOD and PDSOI NSFET structure, possible fabrication process steps, and the TCAD calibration setup. The acquired results have been discussed in Section III, followed by the conclusion in Section IV.

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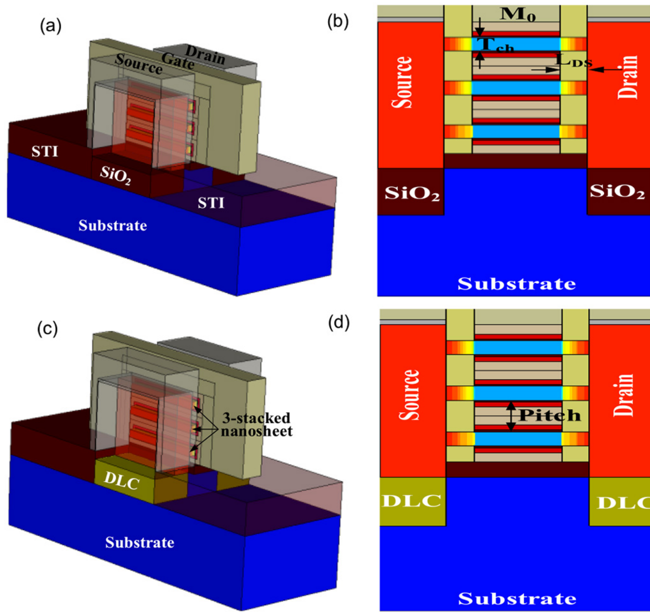


Fig. 1. *3D* schematic and cross-sectional view of (a-b) vertically stacked PDSOI nanosheet transistor; (c-d) vertically stacked PDSOD nanosheet transistor. Here, partially depleted silicon on $SiO_2$ (PDSOI) subsided the leakage current, whereas the partially depleted silicon on crystalline diamond (PDSOD) structure reduces the SHE.

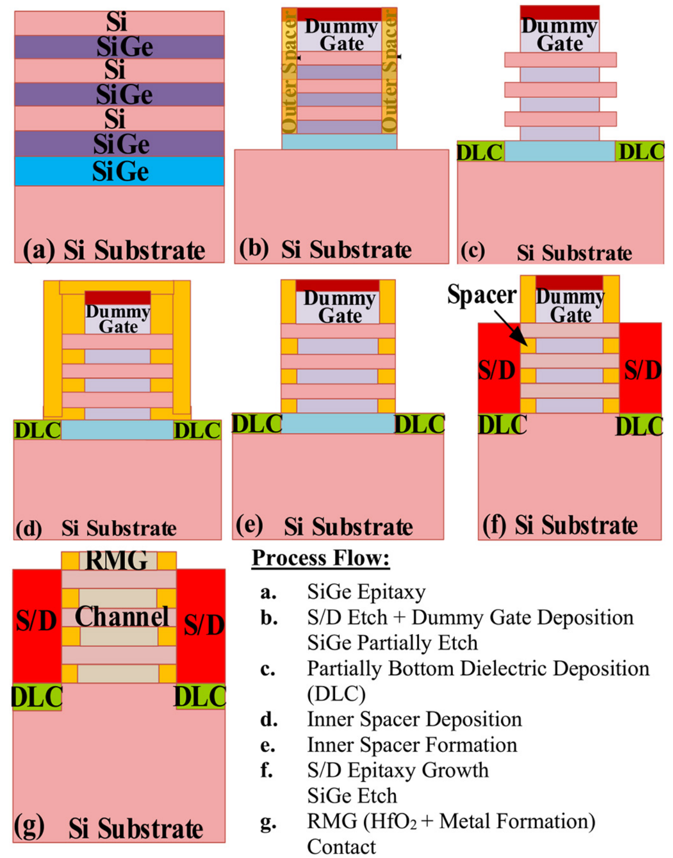


Fig. 2. Shows the process flow explaining the step-by-step approach to realizing the vertically stacked partially depleted silicon-on-diamond nanosheet FET.

## II. Device Structure and Simulation Setup

In this section, we discuss the device structure of NSFET with conventional SOI and proposed SOD layers. We also explain the possible fabrication steps of PDSOI and PDSOD NSFET. In this work, we employed *Sentaurus* TCAD [20] to investigate the electrical characteristics of the nanosheet transistor using well-calibrated TCAD models. This section is sub-divided as follows.

### A. Device Structure of the Proposed PDSOD-NSFET

Fig. 1 shows the schematic of the vertically stacked PDSOI and PDSOD NSFET. The partially buried oxide ($SiO_2$) is replaced with equivalent size high thermal conductivity dielectric material (i.e., crystalline diamond) and placed strategically under the source/drain (S/D) region to mitigate SHE-induced thermal degradation [Fig. 1(c–d)]. The S/D and channel of the NSFET are uniformly doped with an arsenic doping concentration of $2 \times 10^{20}$ $cm^{-3}$ and the boron doping concentration of $1 \times 10^{16}$ $cm^{-3}$, respectively. The S/D extension regions are doped with Gaussian doping to mimic the realistic scenario; due to this, the S/D pads will have graded regions of gradually decreasing conductivity adjacent to the end of the channel. Unless stated otherwise, all the relevant default device parameters are mentioned in Fig. 1 and Table I.

### B. Possible Fabrication Steps of the PDSOD-NSFET

This subsection briefly explains the steps to fabricate the proposed PDSOD NSFET. The step-by-step fabrication flow mentioned in this subsection is similar to [10]. The PDSOD NSFET can be fabricated on the silicon bulk substrate [Fig. 2(a–g)]. Firstly, to implement the partially depleted silicon-on-diamond FET module, the first SiGe layer containing a high % of Ge is grown over the substrate, followed by a stacking layer of low Ge % in SiGe/Si (Fig. 2a).

Dummy gates and spacers are placed before isotropic etching of the SiGe/Si stacked multilayers (Fig. 2b). The Ge %

TABLE I
Parameter Table

| Device Parameter | Value | Unit |
|---|---|---|
| Gate Length ($L_g$) | 12 | nm |
| Channel Width ($t_w$) | 50 | nm |
| Channel Thickness ($T_{ch}$) | 4 -7 | nm |
| Spacer Permittivity | $4\mathcal{E}_0$ | F/cm |
| $HfO_2$ Permittivity (*k*) | $22\ \mathcal{E}_0$ | F/cm |
| Spacer Length ($L_{SP}$) | 5 | nm |
| Interfacial EOT | 0.9 | nm |
| Source/ Drain Doping ($N_{SD}$) | $2x10^{20}$ | $cm^{-3}$ |
| Substrate Doping ($N_B$) | $1x10^{18}$ | $cm^{-3}$ |
| Channel Doping ($N_C$) | $1x10^{16}$ | $cm^{-3}$ |
| S/D Metal Interface Resistance ($R_C$) | $8.4x10^{-10}$ | $\Omega\ cm^2$ |
| **Thermal Properties [21], [22]** | | |
| Gate Metal Conductivity | 0.192 | $WK^{-1}cm^{-1}$ |
| Drain/Source Metal Thermal Conductivity | 1.7 | $WK^{-1}cm^{-1}$ |
| Channel Region Thermal Conductivity | 0.25 | $WK^{-1}cm^{-1}$ |
| Drain/Source Region Thermal Conductivity | 0.62 | $WK^{-1}cm^{-1}$ |
| Oxide Thermal Conductivity ($SiO_2$) | 0.014 | $WK^{-1}cm^{-1}$ |
| High-*k* Thermal Conductivity ($HfO_2$) | 0.023 | $WK^{-1}cm^{-1}$ |
| Silicon Nitride Conductivity ($Si_3N_4$) | 0.15 | $WK^{-1}cm^{-1}$ |
| Crystalline Diamond Conductivity | 20 | $WK^{-1}cm^{-1}$ |

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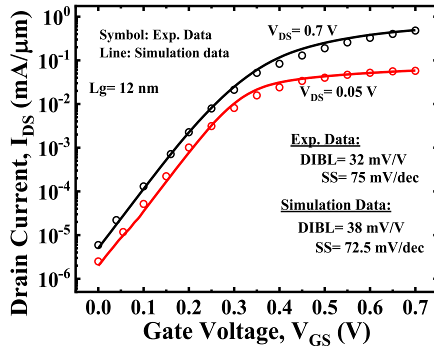


Fig. 3. The calibration of the transfer characteristics ($I_{DS}$-$V_{GS}$) of the partially depleted nanosheet transistor with the experimental data [7].

of the regular SiGe stacked alternative layer should be lower to increase the selectivity between the sacrificial stacked SiGe layers and bottom SiGe. Due to the lowering of Ge % in the alternative SiGe sacrificial stacked layer, the selectivity between the silicon channel layer and alternatively placed SiGe sacrificial stacked-layer will be reduced, resulting in the identification challenge of the active channel region and inner spacer [10]. This sacrificial SiGe stacked layer is removed with very high selectivity material to prevent the nanosheet channel erosion during the process flow of active channel formation. Further, diamond-like-carbon (DLC) is deposited using the plasma immersion ion implantation instead of growing the $SiO_2$ for the PDSOI NSFET, followed by inner spacer deposition [Fig. 2(c–d)] [23], [24]. After DLC deposition, the inner spacer formation and S/D epitaxy are processed [Fig. 2(e–f)]. Finally, after etching out the dummy gate, the formation of gate-oxide, metal gate, and contacts are performed (Fig. 2g).

### C. TCAD Calibration Setup

We have used a 5nm nanosheet transistor for the analysis as a baseline device in this work. The TCAD models are well-calibrated with the experimental data [7] and found a good match (Fig. 3). Further, using well-calibrated TCAD models, we realize the proposed PDSOD NSFET to analyze the electrical characteristics and SHE-induced degradation. We have incorporated the density gradient (DG) model in the simulation framework to capture the channel spatial and electrostatic quantum confinement. Shockley-Read-Hall (SRH) model is used to consider the generation and recombination of the charge carriers. The modified local density approximation model (MLDA) is incorporated into device physics to consider the carrier distribution near the gate oxide/silicon interface. A thin layer mobility model was included to render the mobility degradation of the inversion charge carriers due to quantum confinement of the charge carrier in 5nm thin sheets. The remote phonon and Coulomb scattering models were used to justify the mobility degradation due to high-*k* ($HfO_2$) dielectric with metal (TiN). The vertical field mobility, ballistic mobility, and high field saturation model are used to render the SCEs. The inversion and accumulation layer (IAL) mobility model accounts for effective mobility degradation due to Coulomb scattering, surface roughness scattering, and phonon scattering (temperature dependence) [25]. In this work, the threshold voltage ($V_{th}$) is calculated from the transfer characteristics for a fixed drain-to-source voltage ($V_{DS}$) and extracting at the gate-to-source voltage ($V_{GS}$) value for $I_{DS} = (W_{eff}/L) \times 10^{-7}$, the constant current method [26]. To capture the self-heating effects, we have incorporated the thermodynamic (TH) and drift-diffusion (DD) model-based carrier transport models to accurately capture the behavior of the charge carrier. The S/D electrodes of the nanosheet transistor severely affect the device's ON resistance, which has been considered $8.4\times10^{-10}$ Ω-cm$^2$ in our simulation [31]. The interface thermal resistance of metal-Si has been experimentally extracted, which varies from $1 \times 10^{-5}$ cm$^2$K/W to $1 \times 10^{-3}$cm$^2$K/W [28]–[30]. In NSFET with thickness *h*, acoustic phonon scattering at the boundary interface reduces the mean free path and mass fluctuation scattering due to phonon-dopant impurity [31]. Thus, the thermal conductivity ($k_{th}$) of the Si material is given as [20], [32]:

$$k(z) = k_0(T)\int_0^{\pi/2} \sin^3\theta\left\{1 - \exp\left(-\frac{h}{2\lambda(T)\cos\theta}\right)\cosh\left(\frac{h-2z}{2\lambda(T)\cos\theta}\right)\right\}d\theta \tag{1}$$

where

$$\lambda(T) = \lambda_0\left(\frac{300}{T}\right)nm;\ k_0(T) = \frac{1}{a + bT + cT^2}Wm^{-1}K^{-1}$$

here, $a = 0.03$ K·m/W, $b = 1.56\times10^{-3}$ K$^2$·m/W, and $c = 1.65\times10^{-6}$ K$^3$·m/W, $\lambda$ is temperature-dependent [33], and $\lambda_0$ is 300nm at room temperature (i.e., 300K). $k_0$(T) is the temperature-dependent thermal conductivity. The z-axis is perpendicular to the thin film of the semiconductor (i.e., $T_{ch}$ is chosen along the z-axis). Hence, in our simulation framework, we have used dependent thermal conductivity in NSFET. We have also considered the interface thermal resistance ($R_{th,GSD}$) at the gate, source, and drain contacts $4 \times 10^{-5}$ cm$^2$K/W of the nanosheet FET.

## III. Results and Discussion

In this paper, we investigated the impact of SHE-induced thermal effect on the electrical characteristics of the proposed PDSOD NSFET in comparison to the PDSOI NSFET. The buried $SiO_2$ layer in PDSOI is replaced with a higher thermal conductivity crystalline diamond to reduce the SHE-induced thermal degradation and enhance thermal reliability. Fig. 4(a) depicts the transfer characteristics of PDSOI and PDSOD NSFET without considering SHE. The diamond-like carbon (DLC) is an interesting buried insulator having ~1000 times higher thermal conductivity than $SiO_2$. However, its rough surface prohibits direct bonding to silicon wafers without extensive polishing and surface treatment [34]. Thus, the surface scattering may cause a minor degradation (~1.26%) in the drain current (Fig. 4a) in PDSOD than PDSOI. In Fig. 4(b–d), the impact of SHE is considered on PDSOI and PDSOD NSFET, respectively. Due to SHE, the NSFET cannot perform to its zenith, and the drain current ($I_{ON}$) of the PDSOI NSFET and PDSOD NSFET are degraded by 7.65% (Fig. 4b) and 5.51% (Fig. 4c), respectively.

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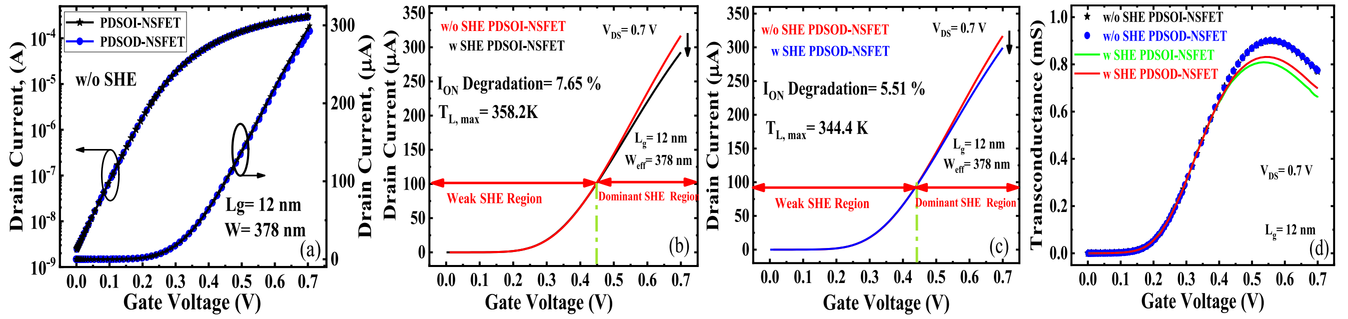


Fig. 4. (a) Shows the transfer characteristics of PDSOI and PDSOD NSFET. PDSOD is realized by using a crystalline diamond in place of the bottom dielectric ($SiO_2$). (b) $I_{DS}$-$V_{GS}$ characteristics of PDSOI NSFET with and without SHE; (c) $I_{DS}$-$V_{GS}$ characteristics of PDSOD NSFET with and without SHE; (d) transconductance ($g_m$) of the PDSOI and PDSOD NSFET with and without SHE.

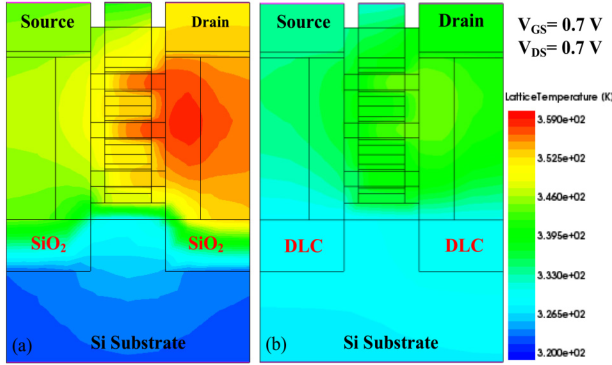


Fig. 5. The contour plot of the device temperature profile in the channel direction shows the hot-spots location of (a) PDSOI NSFET and (b) PDSOD NSFET. Using the crystalline diamond beneath the S/D, the hot spots have been mitigated in the PDSOD NSFET compared to PDSOI NSFET.

Moreover, the calculated intrinsic lattice temperature ($T_L$) of PDSOI and PDSOD NSFET are 358.2K and 344.4K, respectively.The results show that the $T_L$ is improved by 13.8K in PDSOD compared to PDSOI NSFET. It is observed that the effect of SHE-induced thermal degradation on the electrical characteristics of PDSOI NSFET is more than PDSOD NSFET, which has been alleviated by using the higher thermal conductivity dielectric crystalline diamond. Due to this, the transconductance ($g_m$) of the PDSOD NSFET is improved by 2.8% compared to PDSOI NSFET (Fig. 4d), which is a significant improvement for analog/RF performances [35]–[36]. The current degradation ($\Delta I_{degradation}$) of NSFET is calculated by using the formula:

$$\Delta I_{degradation} = \left(\frac{I_{ON} - I_{ON,\ SHE}}{I_{ON}}\right) \times 100\% \tag{2}$$

where $I_{ON}$ and $I_{ON,SHE}$ is the drain current without SHE and with SHE, respectively. In the linear region, the disparity between the $I_{ON}$ of the NSFET is smaller with and without SHE due to the lower power consumption than in the saturation region, which shows that the SHE has a strong dependency on the $V_{GS}$. Fig. 5 shows the spatial thermal contour of the PDSOI and PDSOD NSFET, which explains that in PDSOI NSFET, the hot spots are located at the active (channel) region near the drain. However, in the PDSOD NSFET, the hot spots are shifted towards the silicon substrate resulting in a significant reduction in intrinsic lattice temperature. The influence of the ambient temperature ($T_a$) on the electrical performance ($I_{ON}$, $I_{OFF}$, $g_m$), lattice temperature ($T_L$), and effective thermal resistance ($R_{eff}$) of the NSFET are depicted in Fig. 6. The increase in $T_a$ from 300K to 370K deteriorates the $I_{ON}$, $I_{OFF}$, $g_m$, $T_L$, and $R_{eff}$ by 8.72%, 10.4×, 12.4%, 17.32%, and 8.47%, respectively, in PDSOI-NSFET. The increase in $T_a$ decreases the carrier mobility, resulting in a decrease in NSFET current ($I_{DS}$). However, the SHE-induced thermal degradation can be mitigated in PDSOD NSFET as the $I_{ON}$, $g_m$, $T_L$, and $R_{eff}$ are improved by 2.8%, 2.8%, 3.83%, and 28.12% than PDSOI NSFET.

Due to the crystalline diamond (instead of $SiO_2$ under the S/D), the hot spots have been uniformly located towards the bottom side of the silicon substrate in PDSOD NSFET; thus, it does not allow the heat accumulation in the channel region. Therefore, ambient temperature plays a minor role in the SHE-induced thermal degradation in the PDSOD NSFET. Due to the incessant scaling of the FETs, the current density increases, which enhances the power density allowing the intrinsic lattice temperature to continue increasing, and it will deteriorate the NSFET performance. Fig. 7 shows the impact of varying sheet thickness of NSFET in the interplay of SHE. Our investigation reveals that the sheet thickness considerably impacted the $I_{ON}$, $g_m$, $T_L$, and $R_{eff}$ of the NSFET. Fig. 7(a) shows the variation of drain current with increasing sheet thickness. The drain current of the NSFET increases with sheet thickness due to the enhanced inversion charge density in the increased circumference of the channel region and the less severe impact of the quantum confined mobility degradation of the inversion charge carriers.

This results in higher transconductance ($g_m$) [Fig. 7b]. As the channel thickness increases from 4 to 7 nm, the drain current is increased by 18.86% and 22.1%, and the transconductance is increased by 10.2% and 12.1% in PDSOI and PDSOD NSFET, respectively. Due to the use of crystalline diamond in PDSOD NSFET the SHE is less pronounced, which improves the drain current by 3.22% compared to PDSOI NSFET. Fig. 7(c) shows the variation of lattice temperature and lattice heat flux with varying channel thickness for the PDSOI and PDSOD-NSFET. With increasing the channel thickness, the channel volume-to-surface ratio increases, which

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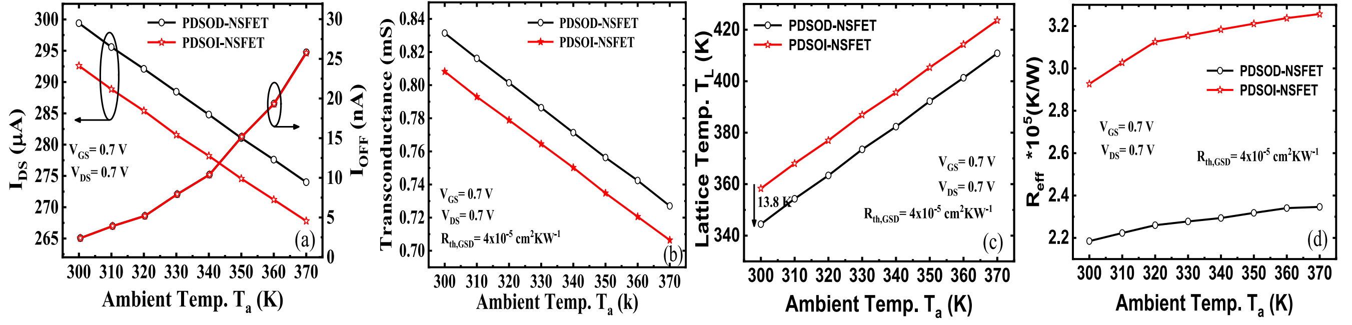


Fig. 6. Impact of varying the ambient temperature on (a) $I_{ON}$ and $I_{OFF}$; (b) transconductance ($g_m$); (c) lattice temperature ($T_L$), and (d) effective thermal resistance ($R_{eff}$) of the PDSOI and PDSOD NSFET. The SHE has been improved significantly in the PDSOD NSFET due to the larger thermal conductivity of the crystalline diamond.

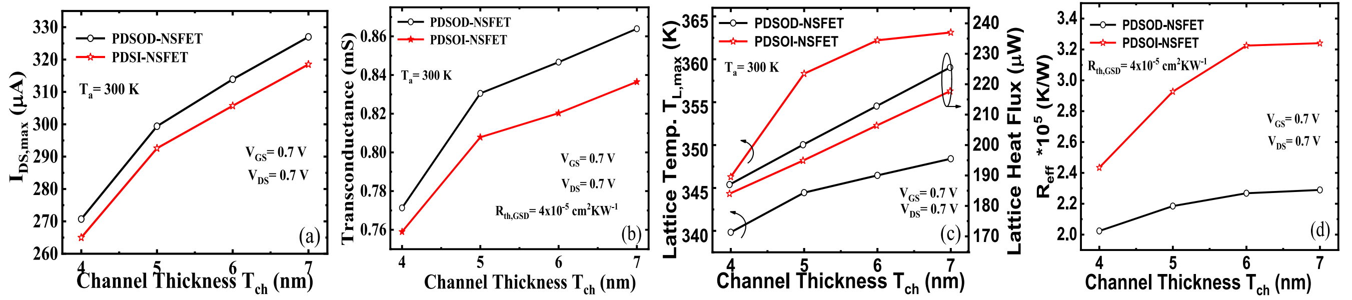


Fig. 7. Impact of varying the nanosheet thickness on (a) maximum drain current ($I_{Dmax}$); (b) transconductance ($g_m$); (c) lattice temperature ($T_L$) and lattice heat flux, and (d) effective thermal resistance ($R_{eff}$) of the PDSOI and PDSOD NSFET. The SHE-induced thermal degradation has been reduced in the PDSOD NSFET due to enhanced lattice heat flux. Increasing the nanosheet thickness enhances the drain current at the cost of thermal degradation.

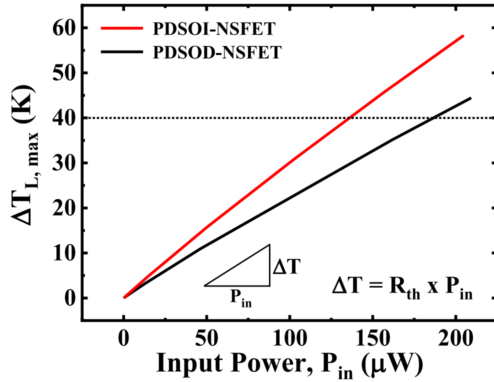


Fig. 8. Effective thermal resistance ($R_{eff}$) of the PDSOI and PDSOD NSFET calculated by the slope of lattice temperature ($\Delta T_L$) difference and the input power ($P_{in}$).

increases the channel current. Therefore, heat is directly assimilated towards the silicon substrate, allowing the active region to remain less vulnerable to SHE in PDSOD NSFET than PDSOI NSFET. Due to this, the lattice temperature in PDSOD NSFET will be improved by ∼4.7% (Fig. 7c). Moreover, the $R_{eff}$ of the PDSOD NSFET is improved by ∼31.25% compared to PDSOI NSFET (Fig. 7d), which shows that PDSOD NSFET has a less severe SHE-induced thermal degradation and has improved thermal reliability. The effective thermal resistance saturates and does not further increase as channel thickness increases. In other words, for the partially depleted NSFET, there exists an optimum value of nanosheet thickness for which the SHE-induced thermal degradation is constant. The $R_{eff}$ of the NSFET is calculated by the slope of the lattice temperature difference and input power, as:

$$R_{\text{eff}} = \frac{\Delta T}{P_{\text{in}}} \quad (3)$$

where $\Delta T = T_{L,max} - T_a$ and $P_{in}$ is the input power.

Fig. 8 shows the maximum lattice temperature versus input power for PDSOI and PDSOD NSFET. The $R_{eff}$ decreases for the PDSOD NSFET as the input power increases at constant lattice temperature, which shows that the heat dissipation path has been shifted towards the substrate. Thus, the crystalline diamond has effectively reduced the SHE-induced thermal degradation by increasing the heat flux rate (Fig. 7c) towards the substrate, allowing the PDSOD NSFET for high-temperature application.

## IV. Conclusion

In this work, we have investigated the self-heating effect (SHE) induced heat removal capability of silicon-on-diamond (SOD) layer on partially depleted nanosheet transistor using the well-calibrated TCAD models. The diamond-like-carbon (DLC) is a higher thermal conductivity material (∼1000 times better than $SiO_2$), which improves the device's thermal reliability. Our analysis reveals that the proposed partially depleted silicon-on-diamond (PDSOD) NSFET has better SHE mitigation capability than the PDSOI NSFET. Using the crystalline diamond, the heat removal path is uniformly shifted from the active (channel) region

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to the silicon substrate in PDSOD NSFET. With varying the ambient temperature from 300K to 370K, the SHE engendered thermal degradation occurs in PDSOI NSFET, such as ON current, transconductance, device lattice temperature, and effective thermal resistance are improved by 2.8%, 2.8%, 3.83%, and 28.12%, respectively, using SOD layer, i.e., in PDSOD NSFET. We have also explored the impact of varying sheet thickness on the electrical characteristics of PDSOI and PDSOD NSFET. It is observed that the thin sheet NSFET shows better and more reliable results. Further, the deterioration in the thermal properties with an increasing channel thickness can be alleviated by using the PDSOD NSFET because it has better thermal reliability.

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