Demonstration of a Nanosheet FET With High Thermal Conductivity Material as Buried Oxide: Mitigation of Self-Heating Effect

Sunil Rathore, Rajeewa Kumar Jaisawal, P. N. Kondekar, and Navjeet Bagga, *Senior Member, IEEE*

***Abstract*— Self-heating-induced thermal degradation is a severe issue in nonplanar MOS architectures. Especially in stacked gate-all-around (GAA) nanosheet FET (NSFET), the self-heating effect (SHE) is a prime concern as the channels are surrounded by low-thermal conductivity material (i.e., a stack of SiO_2 and HfO_2 layers). In this article, through well-calibrated TCAD models, we propose a buried oxide (BOX) engineered NSFET structure, which provides an appropriate heat flow path and mitigates the SHE-induced degradation. Unlike the conventional NSFET, where SiO_2 is kept as a BOX layer, in the proposed NSFET, a crystalline-diamond-like carbon (DLC) is placed ubiquitously beneath the lower sheet, resulting in a reduction in the lattice temperature from the device active region (channel/sheet) toward the DLC substrate. Furthermore, the impact of device geometry, such as channel length (L_g), channel width (T_W), BOX thickness (T_{BOX}), and the number of vertically stacked sheets (N_S), on the thermal and electrical reliability of the proposed device has been investigated.**

***Index Terms*— Effective thermal resistance, nanosheet FET (NSFET), reliability, self-heating effect (SHE), thermal conductivity.**

I. Introduction

TILL date, numerous nonplanar architectures have been reported to satisfy the continuing scaling of semiconductor devices. Among those, the vertically stacked gate-all-around (GAA) nanosheet FET (NSFET) is attained much attention owing to its enhanced electrostatic integrity (ESI) through a surrounding channel/sheet, higher drivability in the same footprint area, better electrical characteristics, and improved short-channel effects (SCEs) compared to the conventional FinFET architectures [1], [2], [3], [4]. However, the electrothermal-induced self-heating effect (SHE) becomes more profound due to the wrapping of the sheets (channels) by a lower thermal conductivity material, i.e., a stack of SiO_2 ($k_{th} = 1.4\ Wm^{-1}K^{-1}$) and high-$k$ HfO_2 ($k_{th} = 2.3\ Wm^{-1}K^{-1}$). This increases the lattice temperature several degrees higher than the ambient temperature. Thus, the NSFET performance and reliability are abysmally affected due to severe phonon boundary scattering (PBS) at the channel and gate dielectric interfaces [5], [6]. Therefore, the analysis and mitigation of the SHE in NSFET are essential to enhance the reliability of the confined geometrical structure. In this regard, punchthrough stopper (PTS) doping is used in conventional bulk NSFET to mitigate the substrate leakage current; however, negative bias-driven band-to-band tunneling (BTBT) becomes a severe issue with this methodology [7]. Thus, NSFET with buried oxide (BOX) layer beneath the source/drain (S/D) pads and sheets could be a potential substitute over its bulk counterpart primarily due to subsiding the subchannel leakage, decreased parasitic capacitance, immunity against process variation, enhanced frequency response, and power performance optimization [8]. Despite the improved performance of the BOX NSFET, the lower thermal conductivity of the BOX (conventionally used SiO_2) prevents the effective heat flow toward the substrate. Therefore, the SHE-induced thermal degradation becomes more palpable in such BOX NSFET, causing the increased lattice temperature, which reduces the device ON current [9].

Thus, to provide a suitable solution, we proposed a novel NSFET structure with the BOX (i.e., SiO_2) replaced by a high thermal conductivity material, i.e., a crystalline diamond-like-carbon (DLC) layer. This provides an adequate heat flow path from the sheets to the substrate owing to the excellent thermal conductivity ($k_{th} = 2000\ Wm^{-1}K^{-1}$), high-field breakdown (10 MV/cm), and low dielectric constant (5.7 ε_0) of DLC, which makes it more suitable for high-frequency and high-power handling applications [10], [11]. Moreover, the fabrication of crystalline DLC as a BOX follows a similar fabrication flow. Thus, DLC-based devices exhibit excellent compatibility with the baseline silicon without altering/degrading the device performance and cross-contamination issues [12]. Furthermore, in this article, we investigated the impact of device geometry, such as channel length (L_g),

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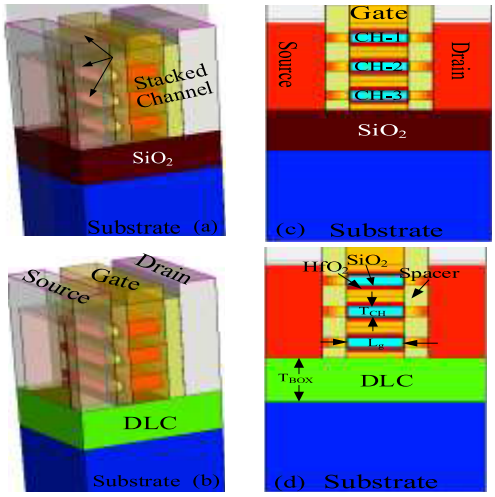

Fig. 1. 3-D isometric view of (a) SiO_2-BOX NSFET, (b) proposed DLC-BOX NSFET and 2-D cross-sectional view of the (c) conventional NSFET with SiO_2 as BOX, and (d) DLC as a BOX.

channel width, BOX thickness (T_{BOX}), and the number of sheets (N_S) on the electrical and thermal characteristics of the proposed NSFET compared to baseline NSFET (i.e., with SiO_2 as BOX). We also analyzed device characteristics with varying ambient temperatures and obtained practical design guidelines considering SHE.

II. Device Structure and Simulation Setup

This section discusses the proposed (i.e., DLC as a BOX) and conventional (i.e., SiO_2 as a BOX) NSFET structures and the simulation framework. We also presented the possible process sequence and a flowchart explaining the fabrication flow of the proposed NSFET structure. The section is divided into three sections as follows.

A. Device Structure and Its Possible Fabrication Flow

The schematic of the proposed and the conventional vertically stacked NSFET structures is shown in Fig. 1. The proposed DLC-BOX NSFET structure is realized by replacing the conventional SiO_2-BOX with a higher thermal conductivity DLC layer placed beneath the S/D and channel region. We considered a three-sheet NSFET as a baseline reference for the analysis, and later, we varied the number of sheets (N_S) for further exploration.

The S/D pads and channels are uniformly doped, whereas the S/D extension regions are rendered with Gaussian doping to mitigate the random doping fluctuations (RDFs) and mimic the realistic scenario [13]. The nitride spacer (Si_3N_4) between the gate and S/D underlap is used. The gate-stack around each sheet comprises a TiN/HfO2/SiO2 layer, at which an interfacial layer of SiO2 (0.6 nm) and high-k HfO2 layer (1.7 nm) with an EOT 0.9 nm is employed [14]. Table I includes all the relevant device parameters used in the simulation and is considered the default unless stated otherwise. Fig. 2 describes the possible process sequence of the proposed DLC-BOX NSFET. The fabrication process of the proposed structure with DLC follows a similar process flow as the baseline reference

TABLE I
Parameter Table

Parameters	Value	Parameters	Value
Gate Length (L_g)	8-50 nm	Channel Width (T_w)	10-50 nm
Channel thickness (T_{CH})	3-7 nm	Substrate doping (N_B)	10^{18} cm^{-3}
Spacer Length (L_{SP})	5 nm	Channel Doping (N_{CH})	10^{16} cm^{-3}
BOX Thickness (T_{BOX})	5-85 nm	S/D doping ($N_{S/D}$)	10^{20} cm^{-3}
Thermal Conductivity ($WK^{-1}cm^{-1}$)			
High-k HfO_2 ($K_{th,\ Hf02}$)	0.023	Gate Metal ($K_{th,\ S/D\ M}$)	0.192
Oxide SiO_2 ($Ksio_2$)	0.014	S/D Metal ($K_{S/D,M}$)	1.7
Spacer ($K_{th,\ Si3N4}$)	0.043	Bulk DLC ($K_{th,\ DLC}$)	20

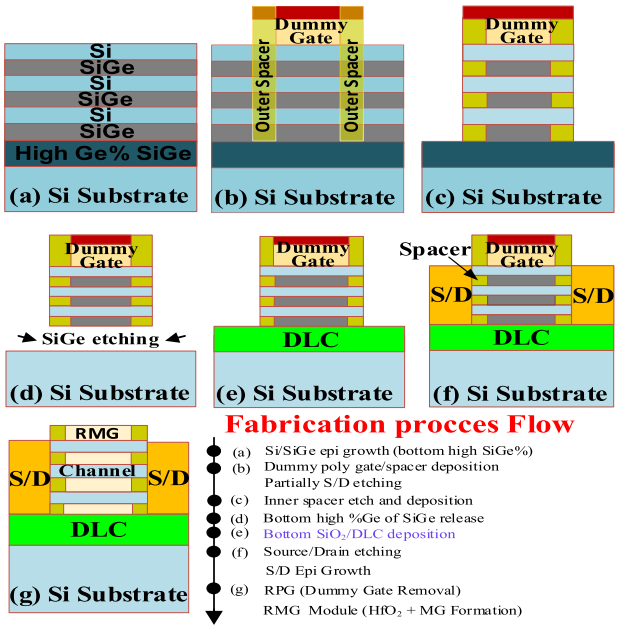

Fig. 2. Possible fabrication process flow of the proposed DLC-BOX NSFET.

NSFET with SiO_2 as BOX [15], [16], [17], along with fewer more steps to incorporate the DLC layer. The process sequence is as follows.

1) The proposed vertical stacked NSFET is grown over the bulk silicon substrate. The fabrication will begin with forming the epitaxy layers of Si/SiGe with varying the mole fraction. A bottom thick SiGe epitaxial layer is grown over a silicon substrate with a higher percentage of Ge [Fig. 2(a)].

2) In the next step, the dummy gate, followed by the gate spacer formation, is performed, similar to the conventional BOX NSFET process flow [8] [Fig. 2(b)].

3) The critical step is to fabricate the inner spacers after the dummy gate depositions for which the partial S/D etching is required. This etching process needs proper attention with high selectivity of Si in SiGe to protect the etching of the bottom thick SiGe layer (i.e., with high Ge%) [8], [17]. Thus, to prevent the failure of forming an inner spacer at the BOX region, dry etching is preferred at this step of the S/D recess [Fig. 2(c)].

4) Furthermore, an S/D recess is needed to expose the bottom thick SiGe layer, followed by etching that layer.

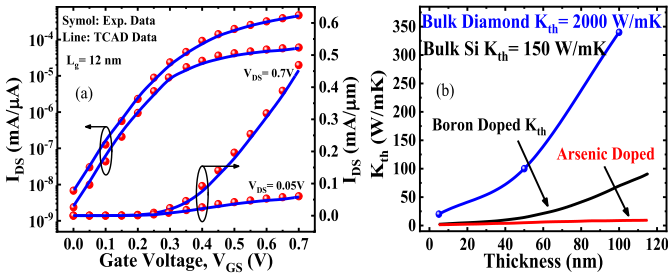

Fig. 3. (a) Calibration of the transfer characteristic (I_{DS}–V_{GS}) of three-stacked NSFET with experiment data [17]. (b) Thickness and doping-dependent experimental thermal conductivity of the silicon and the DLC materials.

In this process, ultrahigh selectivity of silicon is needed to protect the silicon channels/sheets as the silicon channels are exposed to the etchants for a longer time. Therefore, the wet etching technique is preferred [Fig. 2(d)] [18], [19]. Even after removing the complete bottom layer, the structure would not collapse as the sidewall isolation layers supported it.

5) Next, the thin diamond film on the silicon substrate is synthesized using plasma immersion ion implantation and deposition (PIIID) using argon-rich Ar/CH_4 plasma chemistries at 800 °C with radio frequency (RF) power 500 W and pressure of 8×10^{-4} Torr [10], [20] [Fig. 2(e)]. The fabrication of DLC on silicon is compatible with CMOS technology [11], [21]. The acceptor and donor wafers are properly cleaned before the direct bonding, and then, the two wafers are placed with the mirror surfaces facing each other resulting in the direct bonding occurring over the entire surface.

6) Thus, single crystal growth S/D pads are realized after the DLC deposition [22]. Subsequently, an S/D etching is done to remove the undesired contaminants from the S/D region, and then, using conventional methods, the S/D growth and implantation are performed [Fig. 2(f)].

7) Finally, using the replacement poly-gate (RPG) and replacement metal-gate (RMG) module, the proposed NSFET structure with DLC as BOX can be fabricated [Fig. 2(g)].

B. Simulation Setup and Calibration

In this article, we employed the *Sentaurus* TCAD tool [23] to demonstrate the proposed DLC-BOX and conventional (i.e., SiO_2 as a BOX) NSFET structure. The self-consistent drift-diffusion transport equation, charge carrier continuity equation, and Poisson equation are included in the TCAD setup to calibrate the simulated transfer characteristics (I_{DS}–V_{GS}) against the experimental data [17], as shown in Fig. 3(a). The Shockley–Read–Hall (SRH) and Auger models are rendered to capture the doping and temperature-dependent carrier generation and recombination phenomenon. The Slotboom model captures the bandgap narrowing effect due to high doping concentration in the S/D regions. Owing to the high electric field, the Lombardi model, Caughey–Thomas model, and thin layer inversion and accumulation model (IALMob) are used to capture the mobility degradation at silicon-SiO_2 interface caused by remote Coulomb, phonon boundary, surface roughness, and impurity scattering [24]. For low electric field cases, the ballistic model accounts for the quasi-ballistic transport phenomenon [25]. Furthermore, the S/D contacts are wrapped by TiN to reduce the contact resistivity down to 2.1×10^{-9} Ωcm^{-2} [26], [27]. Finally, the threshold voltage (V_{th}) of the standard NSFET is matched by adjusting the gate work function.

C. Thermal Conductivity Setup for NSFET

The conventional drift-diffusion model coupled with the hydrodynamic and thermodynamic models is used to capture the SHE in the proposed NSFET. The Boltzmann transport equation (BTE) with phonon and relaxation time approximation model is used to compute the device's thermal conductivity. In our simulation setup, we used thickness, ambient temperature, and doping-dependent thermal conductivity (k_{th}) variations coupled with the BTE with relaxation time approximation, as explained in our previous publication [28]. The thickness-dependent thin-layer relaxation time ($\tau_{Ly,j}$) is described as follows [29], [30]:

$$\tau_{Ly,j} = \frac{\tau_{B,j}}{1 + \frac{3}{8}\frac{v_j \tau_{B,j}}{r_s d_{Ly}}\left(1 - e\left(-\frac{4n^2W^2}{V_s^2}\right)\right)} \tag{1}$$

where d_{Ly} is the silicon thickness, r_s is constant to modulate the mean free path, and n is the fitting parameter. Table I comprises a list of materials with different thermal conductivities. In general, the thermal conductivity of the DLC is a function of its thickness. The experimental reports show that the conventional BOX thickness lies in 150–300 nm; thus, the DLC's thermal conductivity reduces to 712 $W\text{-}m^{-1}\text{-}K^{-1}$ at 300 K [20]. The DLC acts as a heat sink and provides a heat-flow path, which minimizes the lattice temperature in the active region [21].

Furthermore, the thermal conductivity of DLC depends on the grain boundaries as well as the DLC-silicon interface causes surface roughness, which we have not considered in our simulation. We only included the thickness and temperature-dependent thermal conductivity. The interface thermal resistance of the gate, drain, and source contact is 2×10^{-4} cm^2KW^{-1}, whereas 5×10^{-4} cm^2KW^{-1} is considered for the substrate interface thermal contact resistance [31]. To capture the exact behavior of the SHE in the proposed NSFET, the thermal conductivity values used in our simulation are based on nanosheet width [Fig. 3(b)]. The SHE impacted the lattice temperature, which reduces the mobility and carrier's saturation velocity given as $\mu_{eff} = \mu_0(T_A/T_o)^{-2}$ [32], where μ_{eff} and μ_o are the effective mobility at ambient temperature (T_A) and lattice temperature (T_L), respectively. Thus, this reduction in effective mobility directly influenced the drain current (I_{DS}).

III. Results and Discussion

This section discusses the results of the proposed DLC-BOX NSFET compared to the conventional SiO_2-BOX NSFET obtained using well-calibrated TCAD simulations. The proposed NSFET significantly mitigates the SHE. Furthermore, we discussed the impact of device geometry on SHE-induced thermal degradation. This section is divided as follows.

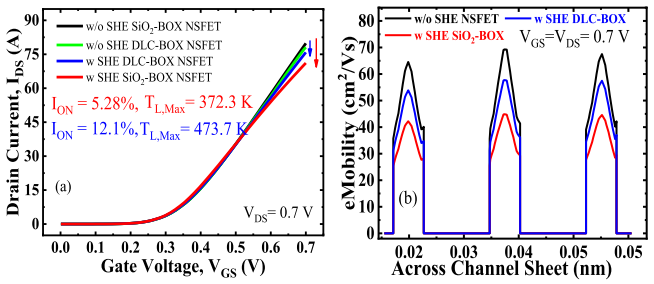

Fig. 4. (a) I_{DS}–V_{GS} characteristics and (b) electron mobility variation of SiO_2-BOX and DLC-BOX NSFET with and without consideration of self-heating effect.

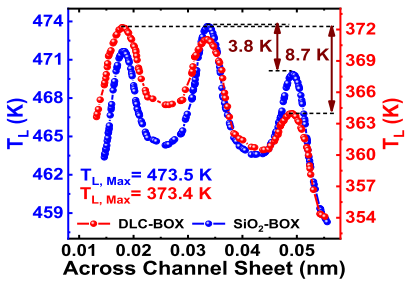

Fig. 6. Maximum lattice temperature ($T_{L,Max}$) variation across the vertically three-stacked NSFET. It is observed that $T_{L,Max}$ significantly reduces using DLC as buried oxide in the proposed NSFET.

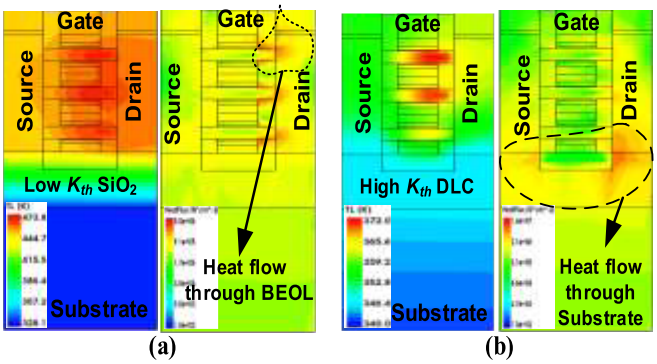

Fig. 5. Contour plot of the lattice temperature and heat flux of (a) SiO_2-BOX NSFET and (b) proposed DLC-BOX NSFET.

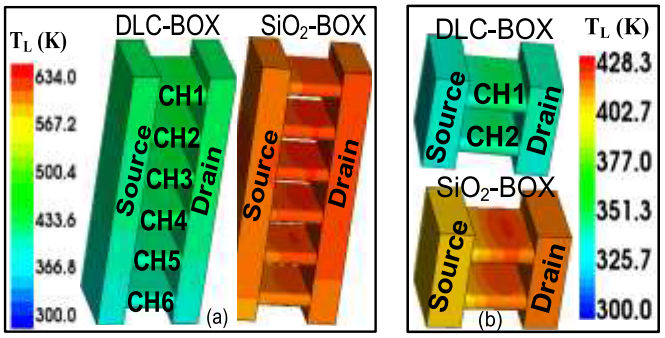

Fig. 7. Temperature distribution (T_L) profile of (a) six-stacked and (b) two-stacked n-channel NSFET with both configurations, i.e., DLC-BOX and SiO_2-BOX.

A. Performance Analysis of the Proposed DLC-BOX and SiO_2-BOX NSFET

To realize the proposed DLC-BOX NSFET, we replaced the conventional SiO_2 BOX layer with a DLC layer of the same thickness. Fig. 4(a) and (b) shows the impact of SHE on ON-current (I_{ON}) reduction and mobility degradation in three stacked DLC-BOX and SiO_2-BOX NSFET and also compares the obtained characteristics without consideration of the SHE. In DLC-BOX NSFET, the current is reduced by 2.1% as compared to SiO_2-BOX configuration due to surface roughness scattering. Furthermore, with consideration of SHE, I_{ON} is degraded by 12.1%, and the maximum lattice temperature ($T_{L,Max}$) increases to 473.7 K for the conventional SiO_2-BOX NSFET. However, in DLC-BOX NSFET, I_{ON} is degraded by ∼5.28%, and $T_{L,Max}$ reaches 372.3K. In DLC-BOX NSFET, the I_{ON} degradation and T_L of the active (channel) region are improved by 56.4% and 21.4%, respectively, over SiO_2-BOX structure due to the alteration of heat flux flow from the active channel region toward the substrate [Fig. 4(b)]. Fig. 5 shows the representative contour plot variation of the lattice temperature and effective heat flux flow path of the SiO_2-BOX and DLC-BOX NSFET.

Due to the use of higher thermal conductivity (k_{th}) DLC material in the proposed NSFET, the effective heat flux flow gets shifted toward the device substrate from the active channel regions. Thus, $T_{L,Max}$ decreases up to 100.1 K. A similar trend is obtained with silicon-on-sapphire used as a BOX layer, which allows the heat flux path and reduces the impact of SHE [33]. In NSFET, mainly hot spots are situated toward the drain/channel interface, and the lattice temperature of the middle channel (CH-2) is higher compared to the upper (CH-1) and bottom channel (CH-3) due to thermal crosstalk. However, the thermal crosstalk reduces using the DLC-BOX, and the heat flux flow path alters from the drain/channel interface toward the device substrate. Fig. 6 shows the effective lattice temperature variation across the three vertical sheets of the proposed and conventional NSFET. It is observed that the bottom channel of DLC-BOX NSFET has ∼8.7 K lower temperature than the top channel due to the usage of high thermal conductivity material, i.e., DLC.

B. Impact of Multistacked NSFET

In this section, we investigated the impact of electrical and thermal characteristics of a multistacked NSFET (varying the number of sheets from 1 to 7). Fig. 7(a) and (b) illustrates the contour profile of T_L for both the structures, i.e., proposed DLC-BOX and SiO_2-BOX NSFET, respectively. The increase in N_S results in thermal crosstalk-induced heat accumulation between the stacked sheets, which periodically enhances the lattice temperature ($T_{L,Max}$) compared to the lower number of stacked channels [Fig. 7(b)]. For $N_S = 6$, the observed value of $T_{L,Max}$ for SiO_2-BOX structure is ∼626 K, which is a way higher than the proposed DLC-BOX NSFET (∼442 K) owing to the heat accumulation among the sheets [Fig. 7(a)]. The accumulation of heat energy hot spots at the channel-drain side in the form of lattice temperature degrades the electrical characteristics. In contrast, the NSFET drivability can be improved by increasing the effective width per footprint

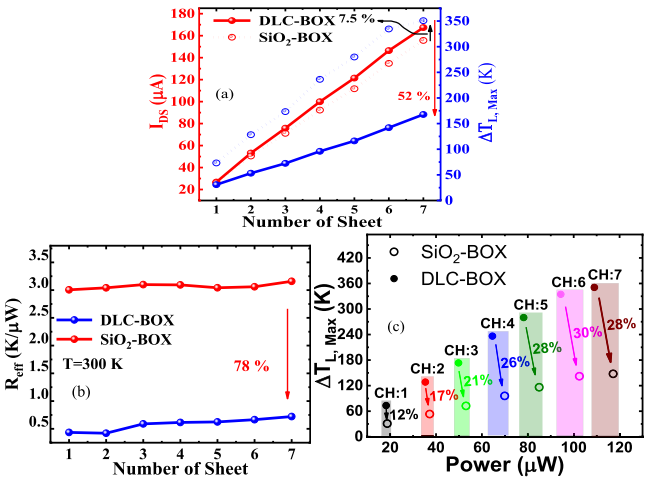

Fig. 8. (a) Drain current and the change in T_L(i.e., $\Delta T_{L,\mathrm{Max}} = T_{L,\mathrm{Max}} - T_A$). (b) Effective thermal resistance (R_{eff}) with varying N_S, and (c) $\Delta T_{L,\mathrm{Max}}$ versus input power of the proposed DLC-BOX and conventional SiO_2-BOX NSFET.

(W_{eff}/footprint), which can be achieved by increasing N_S, as shown in Fig. 8(a). As N_S increases, the drain current (I_{DS}) increases owing to the increase in the effective width $\{W_{\mathrm{eff}} = 2(T_w + T_{\mathrm{CH}})N_{\mathrm{stack}} * N_S\}$, which is a function of N_S. Here, T_{CH} and T_w are the thickness and width of the sheet/channel, respectively. N_{stack} represents the number of the stack. Furthermore, the power dissipation (the energy in the form of heat) is directly proportional to I_{DS}. Thus, for a fixed applied voltage, the lattice temperature would increase with increasing N_S [Fig. 8(a)]. It is observed that, as N_S increases, the "*change*" in lattice temperature (i.e., $\Delta T_{L,\mathrm{Max}} = \mathrm{T_L} - T_A$, with initial $T_A = 300$ K) linearly increases, and for $N_S = 7$, $\Delta T_{L,\mathrm{Max}}$ reaches 350.7 K for the SiO_2-BOX NSFET.

However, the DLC-BOX configuration will provide a heat flow path toward the bottom substrate; hence, $\Delta T_{L,\mathrm{Max}}$ and the effective thermal resistance, $R_{\mathrm{eff}}(=\Delta T_{L,\mathrm{Max}}/P_{\mathrm{in}})$, are improved by 52% and 78%, respectively, which improves I_{DS} by 7.5% [Fig. 8(a) and (b)]. Fig. 8(c) shows the variation of $\Delta T_{L,\mathrm{Max}}$ with dc input power for both configurations by varying N_S at fixed drain bias ($V_{\mathrm{DS}} = 0.7$ V). As $N_S$increases, the high phonon scattering occurs at the semiconductor (channel) and low thermal conductivity dielectric interface, which enhances the lattice temperature. However, using the DLC-BOX in the proposed NSFET, the thermal crosstalk between the stacked nanosheets decreases, which decreases $\Delta T_{L,\mathrm{Max}}$ and makes it almost constant for the higher N_S. Thus, the dc power improves due to improved I_{DS} at a constant V_{DS}.

C. Impact on Ambient Temperature on NSFET

The scaling of the device enhances the current density and average temperature of the integrated chip (IC); thus, the electrical and thermal characteristics of the device severely degrade. We investigated the impact of varying ambient or atmospheric IC temperature (T_A) on the performance of the proposed DLC-BOX and baseline SiO_2-BOX NSFET. As T_A increases, the lattice temperature ($T_{L,\mathrm{Max}}$) increases from 473.7 to 567.9 K, which decreases the device saturation drain

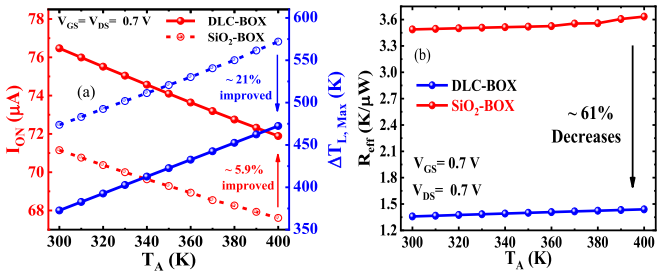

Fig. 9. Impact of ambient temperature (T_A) on (a) I_{DS} and $T_{L,\mathrm{Max}}$ and (b) R_{eff} of the proposed DLC-BOX and SiO_2-BOX NSFET.

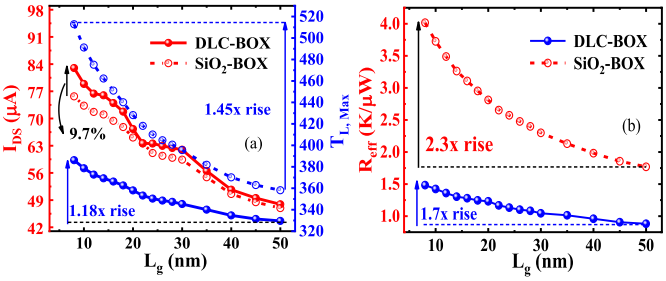

Fig. 10. Impact of channel length scaling on (a) I_{DS} and $T_{L,\mathrm{Max}}$ and (b) R_{eff} of the proposed DLC-BOX and SiO_2-BOX NSFET.

current from 77.1 to 67.61 μA (12.31% decrease) in SiO_2-BOX NSFET. However, using the DLC as a BOX, the T_L and R_{eff} are improved by 21% and 61%, respectively, which improves the saturation drive current by 5.9% (Fig. 9).

D. Impact on Dimensional Variations of the NSFET

A thorough discussion in the previous subsections reveals that the electrical characteristics (i.e., especially I_{DS} or I_{ON}) of NSFETs are significantly affected by the SHE. Thus, careful device geometrical optimization, such as NSFET thickness and width, is a prime concern because, in the nanoscale regime, the thermal conductivity (k_{th}) is affected by these device geometrical parameters. The k_{th} variation impacted the SHE and its induced thermal degradation, thus, the device's performance and reliability. Therefore, we investigated the prime objectives, such as the impact of channel length (L_g), sheet width (W_{eff}), and BOX thickness (T_{SUB}) on lattice temperature ($T_{L,\mathrm{Max}}$), ON current (I_{ON}), and effective thermal resistance (R_{eff}). Fig. 10 shows the channel length scaling from 50 to 8 nm on I_{ON}, $T_{L,\mathrm{Max}}$, and R_{eff} of the proposed DLC-BOX and SiO_2-BOX NSFET. Reducing L_g increases I_{ON}; however, the increase in the lateral electric field causes high energetic charge carriers that create hot spots at the channel/drain interface and increase the lattice temperature and effective thermal resistance of the NSFET. However, using the DLC-BOX in NSFET, the electrical and thermal characteristics can be improved significantly [Fig. 10(a) and (b)]. I_{ON}, $T_{L,\mathrm{Max}}$, and R_{eff} are improved by 9.7%, 25.5%, and 62.5% in the proposed DLC-BOX NSFET compared to the SiO_2-BOX NSFET at $L_g = 10$ nm. Increasing W_{eff} in NSFET enhances the current drivability of the device, hence the maximum lattice temperature variation ($T_{L,\mathrm{Max}}$). As W_{eff} increases from 100 to 350 nm, $T_{L,\mathrm{Max}}$ increases by 44.45%

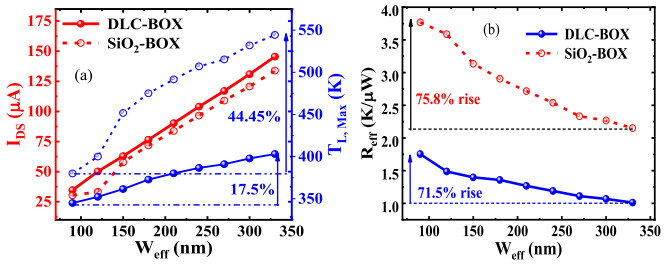

Fig. 11. Impact of effective width scaling on (a) I_{DS} and $T_{L,Max}$ and (b) R_{eff} of the proposed DLC-BOX and SiO_2-BOX NSFET.

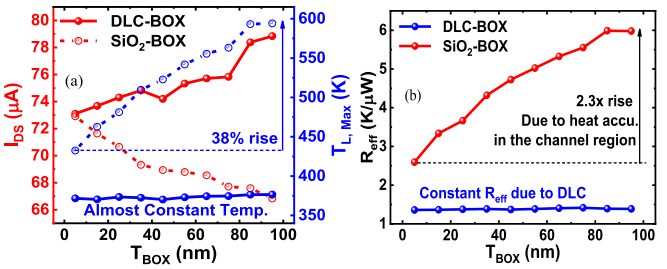

Fig. 12. Impact of T_{BOX} on (a) I_{DS} and $T_{L,Max}$ and (b) R_{eff} of the proposed DLC-BOX and SiO_2-BOX NSFET.

TABLE II
COMPARISON TABLE

Parameters	SiO_2 BOX NSFET	Bulk NSFET	DLC BOX NSFET
Lattice Temperature (T_L)	473.5 K	387.7 K	372.3 K
ON Current (I_{ON})	71.15 μA	74.98 μA	75.85 μA
OFF Current (I_{OFF})	0.501nA	1.87nA	0.501nA
Power Consumption (P)	49.81μW	52.48μW	53.1μW

and 17.5% in SiO_2-BOX and DLC-BOX NSFET, respectively. However, narrower sheet width decreases the current drivability of the device due to enhanced R_{eff} due to reduced heat path. Consequently, owing to improved T_L in the DLC-BOX NSFET, I_{ON} enhanced by 8.6%, which decreases R_{eff}. Thus, by narrowing W_{eff} from 350 to 100 nm, R_{eff} increases by 75.8% and 71.5% in DLC-BOX and SiO_2-BOX NSFET, respectively [Fig. 11(a) and (b)]. This is because the thermal conductivity of the NSFET has device dimensions dependency. Thus, channel length and sheet width play a decisive role in the thermal characteristics of the NSFET. Apart from the BOX thermal conductivity, the DLC layer's thickness (T_{BOX}) also has a significant role, as shown in Fig. 12. The BOX thickness-dependent lattice temperature variation can be given as

$$T_{L,\mathrm{Max}} = (P \times T_{\mathrm{BOX}}/\mathrm{K_{th}} \times A) \tag{2}$$

where P is the effective power generated in the channel, and A is the effective area of the channel. Increasing T_{BOX} in the baseline structure further hinders the heat flux flow from the active (sheet) area to the substrate; thus, it increases the lattice temperature. Therefore, it decreases the drive current of the SiO_2-BOX NSFET [Fig. 12(a) and (b)].

However, in the case of DLC-BOX, the thermal conductivity increases with the layer thickness [Fig. 3(b)]. Moreover, we compared results with bulk NSFET (Table II), which signifies that the deterioration of the electrical and thermal characteristics can be significantly mitigated by using the proposed DLC-BOX architecture. Thus, the proposed DLC-BOX NSFET, with its dimensional variability, is worth exploring to obtain a reliable NSFET operation.

IV. CONCLUSION

The crux of this article is the proposal and demonstration of a novel NSFET by replacing the BOX layer with a high thermal conductivity material, which mitigates the SHE-induced performance degradation. A crystalline DLC layer is incorporated in the place of the conventional SiO_2 layer to realize the proposed DLC-BOX NSFET. DLC has higher thermal conductivity than SiO_2, which provides a suitable heat flow path from the active (channel/sheet) region to the substrate and thus reduces/shifts the hot spots toward the substrate. Through extensive well-calibrated simulations, we analyzed the thermal and electrical characteristics of the proposed DLC-BOX NSFET and compared the results with the baseline conventional NSFET, i.e., SiO_2 as BOX. Furthermore, the impact of the device geometrical variation, such as channel length (L_g), sheet width (W_{eff}), BOX thickness (T_{BOX}), and the number of sheets (N_S) on device performance, has been investigated. In conventional SiO_2-BOX NSFET, the BOX thickness hinders the heat flow, whereas the thickness-dependent thermal conductivity modulation in DLC provides an additional advantage to reduce the lattice temperature. The results show that SHE-induced lattice temperature and current degradation are improved by 21.4% and 56.4% in the proposed DLC-BOX NSFET compared to baseline SiO_2-BOX NSFET. Moreover, we also evaluated the performance under the influence of varying ambient temperatures and provided a detailed insight into SHE-induced thermal degradation. Hence, the presented work proposes a possible and viable solution to mitigate the self-heating in stacked nanosheet transistors.

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