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Role of temperature on linearity and analog/RF performance merits of a negative capacitance FinFET

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Abstract

Temperature plays a decisive role in semiconductor device performance and reliability analysis. The effect is more severe in a negative capacitance (NC) transistor, as the temperature modulates the ferroelectric polarization, implicitly included by the Landau coefficients (α, β, γ) in Technology Computer Aided Design (TCAD) simulations. In this paper, through TCAD simulations, the role of varying ambient temperature is investigated in the linearity and analog/radio-frequency (RF) merits of NC-FinFET. The varying temperature modulates the carrier mobility, the semiconductor bandgap, and the Landau parameter (α). We analyzed the analog/RF and linearity metrics, such as total gate capacitance (C_{gg}), transconductance (g_m), unity gain cut-off frequency (f_T), the transconductance-frequency product, gain-bandwidth product, higher-order transconductance (g_{m2} and g_{m3}), voltage intercept points, third-order power intercept and intermodulation points, and 1 dB CP using well-calibrated TCAD models. Our analysis reveals that these parameters are strongly dependent on temperature and the NC span (defined by using S-curve) shrinks with the rise in temperature. Finally, a source follower and three-stage ring oscillator are designed to test the frequency compatibility of the AC simulation for varying temperatures.

Keywords: negative capacitance, doped-HfO_2, FinFET, analog/RF, linearity, transconductance

(Some figures may appear in colour only in the online journal)

1. Introduction

FinFET-based logic devices offer enhanced gate electrostatic, which profoundly reduces the short channel effects and paves the path for improved performances and low power dissipation CMOS circuits over conventional MOSFETs [1–4]. However, the Boltzmann tyranny still put the fundamental constraint on a subthreshold swing (SS), i.e. 60 mV decade^{-1} at 300 K (i.e. room temperature), due to a similar operation phenomenon in FinFETs. This hinders the scaling of the supply voltage and, in turn, power, which obstructs the high-frequency applications. Therefore, to further increases the operational frequency, we need to scale the supply voltage, keeping power density constant. Thus, to reduce the V_{DD}, we need to scale the SS without altering the fundamental physics of the transport mechanism. To realize such a steep slope device, the negative capacitance (NC) phenomenon is one of the alternatives, obtained by placing a ferroelectric (FE) layer at the gate stack in series with the conventional interfacial oxide (SiO_2). Therefore, the FE layer provides an internal voltage amplification due to the stabilized NC effect [5]. This bestows the steep slope characteristics (i.e. SS < 60 mV decade^{-1}), higher ON current (I_{ON}), and improved switching speed compared to the baseline (BL) FET [5–9]. However, in the nanoscale devices, employing

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the conventional perovskite materials as a FE layer was challenging due to poor compatibility with CMOS fabrication flow. Thus, the concept of realizing a thin-layer doped-HfO_2 layer as an FE layer is a breakthrough, which established the dominance of NC-based devices for the leading-edge future advanced technology node compared to conventional FET [10, 11]. The doped-HfO_2 layer with specific dopants offers significantly high remanent polarization (i.e. up to 45 μC cm^{-2}) and a large coercive electric field ($\sim$1–2 MV cm^{-1}) [12]. The FE properties of the doped-HfO_2 layer can be implemented in Technology Computer Aided Design (TCAD) simulation using the L–K equation with adequately tuned Landau parameters (α, β, γ, g, ρ). A thorough investigation of such parameters is required for a reliable NC operation. The temperature is the most significant factor that modulates the Landau parameters. Out of such relevant Landau parameters, predominately 'α' is strongly affected by variation in the temperature [13], which in turn changes the NC property, i.e. the span of the S-curve. Apart from the NC property, the temperature significantly affects the other device characteristics such as mobility, bandgap, etc. Therefore, the governing analog merits are affected by the temperature.

In general, higher transconductance and lower output conductance (g_d) are essential requirements for high data transfer in the high-frequency range (i.e. 95 GHz–3 THz) [14–16]. In such high-frequency applications, the impact of temperature needs rigorous investigation as the modulation in these parameters puts severe questions for reliability. The linearity of the device at such high frequencies also requires precise attention, which is derived using fundamental analog merits, e.g. g_{m2}, g_{m3}, voltage intercept point (VIP_2), etc. Thus, the overall impact of temperature needs to be addressed for a device used for analog applications.

In this paper, we have chosen the NC-FinFET as a BL device and thoroughly investigated the impact of varying ambient temperatures from 250 K to 350 K on analog/radio-frequency (RF) and linearity metrics. The following are the *key contributions* to this paper:

(a) Analyzing the impact of temperature on Landau parameter (α) of the Si-doped HfO_2, which plays a decisive role in DC characteristics, S-curve, etc.
(b) Investigation of varying temperatures on analog/RF merits such as g_m, intrinsic gain, C_{gg}, f_T, gain-bandwidth product (GBP), and transconductance frequency product (TFP) of the NC-FinFET.
(c) Investigation of impact of temperature on Linearity performance using the performance metrics such as gm_2, gm_3, VIP_2, VIP_3, intermodulation distortion (IMD_3), 1 dB compression point (CP), and input intercept point (IIP_3), etc.
(d) Designing of a common source (CS) amplifier and a three-stage ring oscillator (RO) using mixed-mode simulation.

The paper is arranged as follows: section 2 deals with the device structure and TCAD simulation framework. The results of our study are presented in section 3. Finally, section 4 concludes the manuscript.

2. Device structure and TCAD setup

Figure 1 shows the schematics of the BL FinFET (figure 1(a)), MFM capacitor (figure 1(c)), and NC-FinFET (figure 1(e)). The NC-FinFET is realized by placing a doped-HfO_2 FE-layer at the gate stack of the BL FinFET. SiO_2 is an interfacial layer in the gate stack with a thickness of 0.55 nm. The doped HfO_2 layer (in NC-FinFET) or high-k gate dielectric (in BL FinFET) of 1.7 nm is considered to calibrate the simulation data with experimental results, reported an effective EOT of 0.85 nm [3]. The choice of the doped-HfO_2 FE layer will also provide the area overhead compared to BL FinFET. A 14 nm industry-standard silicon-on-insulator FinFET is chosen as a reference BL, which is well-calibrated using *Sentaurus* TCAD [17] against the experimental data. Uniform phosphorus doping in S/D pads and boron doping in the channel region is employed. In the recessed S/D extension region Gaussian doping profile is used to minimize the random dopant fluctuations. All the relevant parameters used in the simulation are mentioned in table 1 unless stated otherwise. In TCAD simulation, the drift-diffusion models coupled with quantum potential are used to support the charge carrier transport. Doping and temperature dependant recombination models, such as SRH and Auger are employed to account for carrier generation and recombination. For high-field saturation, the Caughey-Thomas model is considered. Lombardi and ballistic mobility models are included to consider the mobility degradation due to high-k dielectric. Moreover, the doping-dependent (UniBo) mobility model is incorporated for the electron–hole and lattice scattering [18]. At last, the gate metal work function is tuned to match the I_{DS}-V_{GS} characteristics of the simulated results against the experimental results (figure 1(b)).

Further, the FEPolarization model (to solve the L–K equation) coupled with the calibrated BL FinFET device physics is incorporated into the device physics section of the TCAD to obtain the requisite NC characteristics. In our simulation study, the Si-doped HfO_2 layer is used as FE material, with a remanent polarization (P_r) and coercive field (E_C) of 10 μC cm^{-2} and 1 MV cm^{-1}, respectively [10]. The static Landau coefficients: $\alpha = \frac{-3\sqrt{3}}{4}\frac{E_c}{P_r}$, $\beta = \frac{3\sqrt{3}}{8}\frac{E_c}{P_r^3}$, and γ are extracted by fitting the experimental P–E (polarization vs. electric field) curve, as shown in figure 1(d). The impact of incorporating the FE material in the gate stack (to realize NC-FinFET, figure 1(e)) on the transfer characteristics is shown in figure 1(f), which demonstrates the drain current and the SS are improved by $\sim$30% and $\sim$11%, respectively. At last, to provide the frequency compatibility of the realized NC-FinFET, we have designed a single-stage CS amplifier with the resistive load (R_D) and three- RO using mixed-mode simulation in *Sentaurus* TCAD itself. In the transient analysis for the mixed-mode AC simulation framework, the 3*D* device structure in the circuit netlist is coupled using the Sentaurus TCAD (*Sdevice*).

3. Results and discussion

This section discussed the impact of the rise in ambient temperature from 250 K to 350 K on the electrical, linearity,

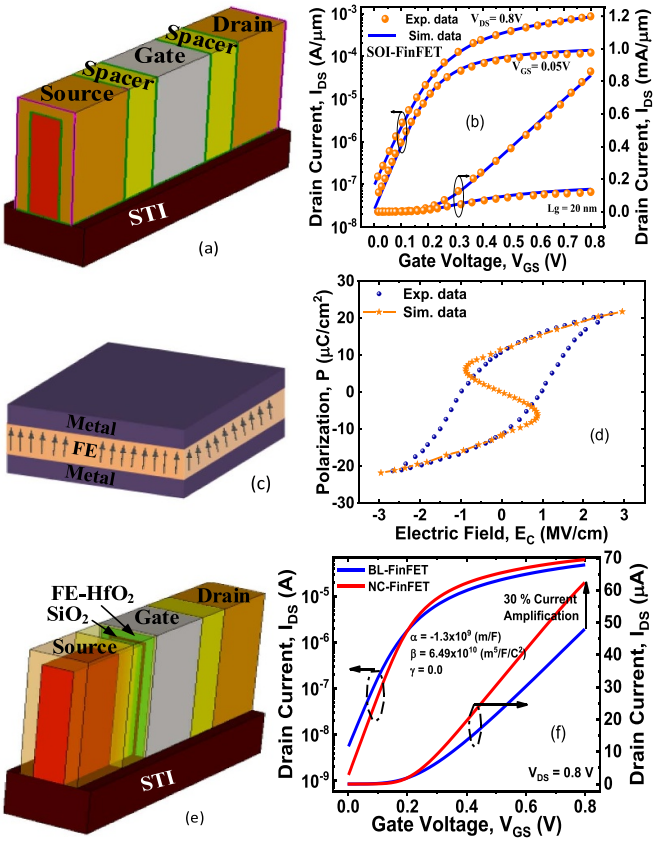

Figure 1. (a) *3D* schematic of baseline (BL) FinFET; (b) calibrated transfer characteristics (I_{DS}–V_{GS}) with the experimental data [3], which shows a good match in simulation and experimental data; (c) a Metal-FE-metal capacitor, simulated to match the S-curve (d); (e) the NC-FinFET is realized by employing an FE-layer at the gate stack of the BL FinFET; (f) NC-FinFET shows ∼30% improvement in I_{ON} as compared to BL FinFET.

Table 1. Parameter table.

Parameters	Value
Gate length (L_G)	20 nm
Height of Fin (F_h)	26 nm
Width of Fin (F_w)	6.5 nm
Equivalent oxide thickness (EOT)	0.85 nm
Spacer length (L_{SP})	8 nm
Source/Drain doping (N_{SD})	10^{20} cm^{-3}
Channel doping concentration (N_{ch})	10^{16} cm^{-3}
Thickness of shallow trench isolation (T_{STI})	10 nm

and analog/RF performance characteristics of the NC-FinFET. Further, we have also investigated the effect of the varying ambient temperature on the output characteristics of the CS amplifier and a three-RO designed using NC-FinFET.

3.1. Impact of temperature on L–K parameters

The temperature plays a significant role in modulating the device characteristics. Temperature does not only modulate

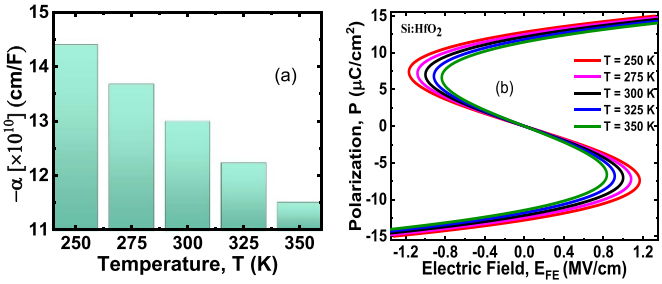

Figure 2. (a) The impact of increasing the temperature on α varies linearly. This results in the shrinkage of the span of the NC region; (b) accordingly, S-curve changes for different values of α due to varying temperature for the Si-doped HfO_2 FE layer.

the intrinsic properties of the BL but also impacts the Landau parameter (more significantly to α), which governs the NC property of the FE-layer. The ferroelectricity arises due to the unique electric field (E_{fe}) and polarization (P) relation of the FE material, which can be modeled by using the Landau-Khalatnikov (L–K) expression [9, 19] given as follows:

$$E_{fe} = \frac{V_{fe}}{T_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho\frac{\partial P}{\partial t} - 2g\Delta P \qquad (1)$$

where α, β, and γ are the static Landau FE material-dependent coefficients. Here, α is strongly affected by the temperature and varies as follows, according to the Curie law; however, the impact of temperature variation on β and γ is negligible [13]:

$$\alpha = \alpha'_x \times 10^{10}\,(T - T_c)\,. \qquad (2)$$

T_C is the Curie temperature and is taken as 750 K for the Si-doped FE material. Here, α'_x is the positive static Landau coefficient. As the temperature increases, the value of 'α' decreases due to decreases in the values of the coercive electric field (E_c), and the span of the NC region shrinks, which ultimately alters the S-curve (figure 2(b)). In addition, under quasi-static uniform domain analysis, we considered the default values of ρ (=2.25 × 10^{-4} Ω cm), the FE damping constant, and $g = 1 \times 10^{-4}$ cm^3 F^{-1}, which is the coupling coefficient. In equation (1), V_{fe} and T_{fe} represent the voltage drop and thickness of the FE layer, respectively. For small voltage (V_{fe}) applied across the FE material, the electric displacement or gate charge density (Q_g) and FE polarization (P) can be expressed by applying the boundary condition across the metal-FE interface as:

$$P \approx Q_g - \varepsilon_0\varepsilon_r E_{fe}. \qquad (3)$$

Sentaurus TCAD solves self-consistently electrostatic of the Poisson equation and single domain L–K equation by combining equations (1)–(3) to obtain V_{fe} as a function of the gate charge density. The values of L–K parameters used in the simulation are: $\alpha = -1.3 \times 10^{11}$ cm F^{-1}, $\beta = 6.49 \times 10^{20}$ cm^5 F^{-1} C^{-2}, and $\gamma = 0.0$ cm^9 F^{-1} C^{-4}.

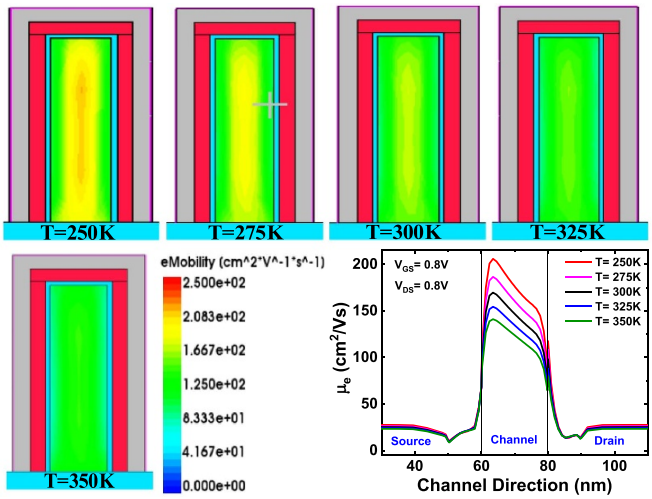

Figure 3. Contour plot to represent the impact of rising temperature on electron mobility at different temperatures ranging from 250 K to 350 K. Increasing the temperature decreases carrier mobility.

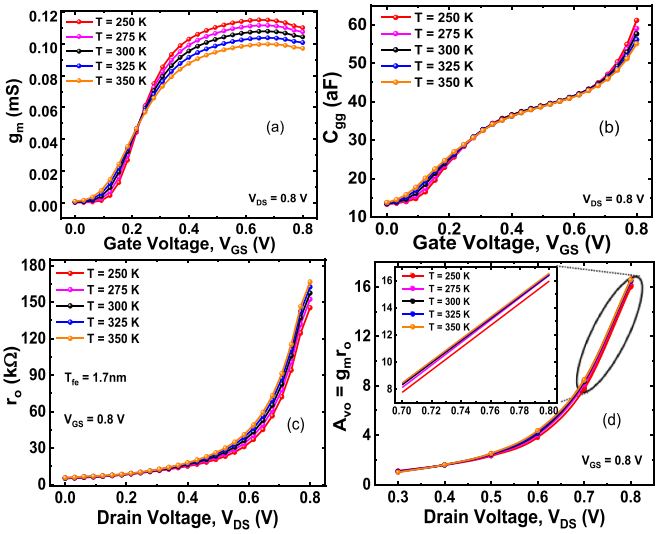

Figure 4. Impact of increasing temperature on (a) transconductance (g_m), (b) total gate capacitance (C_{gg}), (c) output resistance (r_o), and (d) intrinsic voltage gain (A_{vo}). Increasing the temperature enhances the A_{vo} due to an increase in the value of r_o with the rising temperature. however, the values of g_m and C_{gg} decrease with increasing temperature.

3.2. Impact of temperature on intrinsic behavior of baseline FinFET

The change in temperature significantly affects the device's intrinsic factors, i.e. carrier mobility and the bandgap of the material. The mobility and the bandgap are strongly governed by the temperature as [20, 21]:

$$\mu_{\text{eff}} = \mu_{\text{eff}\,0}\left(\frac{T}{T_0}\right)^{-2} \tag{4}$$

where T_0 is the room temperature, and T is the lattice temperature. $\mu_{\text{eff}\,0}$ and μ_{eff} are obtained at room temperature and lattice temperature, respectively:

$$E_{\text{BG}}(T) = E_{\text{BG}}(T_0) - \frac{AT^2}{T+B} \tag{5}$$

where E_{BG}(To) is considered as 1.16 eV, $A = 4.73 \times 10^{-7}$ eV K^{-1}, and $B = 636$ K for Si material. From (equations (4) and (5)), it can be concluded that increasing the temperature decreases both the carrier mobility (figure 3) and energy bandgap, ultimately deteriorating the various electrical characteristics of BL FinFET. Figure 3 depicts the variation of the carrier mobility along the channel direction in an *n*-type NC-FinFET during the ON state. The device operation holds a similar mechanism of barrier lowering as in conventional MOSFET. Due to higher doping in the S/D regions, the mobility of the charge carrier is significantly small.

However, the channel doping concentration (in other words, the inversion carrier concentration in the ON state) is smaller than the S/D doping. Thus, a sharp increase in mobility is observed in the channel region compared to the S/D regions. Further, in the channel region, the charge comes under the vicinity of the vertical (due to V_{GS}) and horizontal (due to V_{DS}) electric field components. Thus, the mobility graph shows a declining slope towards the drain end due to the higher impact of the horizontal component at the drain side.

Now, as we increase the temperature, the lattice scattering increases [18, 21], reducing mobility, which can be explained using equation (4). Therefore, the combined effect of the temperature on both intrinsic (i.e. BL property) and extrinsic factors (i.e. on FE properties) put significant constraints on NC-FinFET characteristics employed in analog/RF and linearity analysis as discussed in the following sub-sections.

3.3. Effect of varying temperature on analog/RF merits of NC-FinFET

Transconductance is indeed a key parameter determining the drain current variation by varying the gate voltage (V_{GS}) with keeping the drain voltage (V_{DS}) constant. The high value of transconductance is essential for better analog/RF merits and gain of any FET-based circuit. Mathematically it is given as [2]:

$$\text{g}_{\text{m}} = \frac{\text{d}I_{\text{DS}}}{\text{d}V_{\text{GS}}}. \tag{6}$$

The effect of temperature on transconductance is shown in figure 4(a). Increasing the temperature decreases the transconductance of the device in the moderate to strong inversion region because the carrier mobility decreases due to the scattering phenomenon. Further, the increase in V_{GS} decreases the transconductance due to severe scattering phenomenon occurring at high gate voltage (in strong inversion region). However, in the subthreshold region, increasing the temperature increases the transconductance of NC-FinFET due to the dominance of the energy band gap narrowing compared to the mobility degradation. The increase in temperature from 250 K to 350 K causes the energy band gap to decrease (equation (5)), and due to this, more charge can transfer from the valence

band to the conductance band, which enhances the transconductance in the subthreshold regime. The increase in the gate voltage (V_{GS}) increases the internal voltage amplification due to NC property of the FE layer; thus, the channel charge increases. Therefore, the total gate capacitance (C_{gg}) increases with V_{GS}, as shown in figure 4(b) [8, 9]. Here C_{gg} is the series combination of FE layer and SiO_2 layer capacitances. Further, we analyzed the impact of temperature on C_{gg}, which shows the opposite trend in subthreshold and strong inversion regions with varying temperatures. In the subthreshold region, the voltage across the FE layer (i.e. V_{fe}) is small enough to impact the capacitance matching significantly. Thus, the intrinsic characteristics of the device severely play a role in defining the impact of temperature. Therefore, the increase in temperature from 250 K to 350 K causes bandgap narrowing (equation (5)), which enhances total gate capacitance (figure 4(b)) of the NC-FinFET in the subthreshold regime. However, with an increase in V_{GS}, the V_{fe} also increases, and C_{fe} changes significantly. The increase in temperature changes the slope of the S-curve, i.e. C_{fe} (figure 2(b)). Thus, this change in C_{fe} alters the capacitance matching between C_{fe} and C_{ox}, which in turn decreases the C_{gg} with increasing temperature in the strong inversion regime (figure 4(b)). Thus, the electrical characteristics, such as g_m and C_{gg} of the NC-FinFET deteriorates with the temperature increases,, as shown in figures 4(a) and (b). However, the output resistance (r_o) improves while increasing the temperature, which improves the intrinsic gain (A_{vo}) of the NC-FinFET device (figures 4(c) and (d)). Therefore, the intrinsic gain of the NC-FinFET continuously increases for the fixed V_{GS}. Using the doped HfO_2 in the gate stacked, the deterioration in the electrical characteristics is mitigated compared to the BL FinFET. The frequency at which the gain of the FETs reaches the unity value is defined as the unity gain cut-off frequency (f_T), given as [22, 23]:

$$f_T = \frac{g_m}{2\pi x C_{gg}} \tag{7}$$

where C_{gg} is the total gate capacitance defined as $C_{gg} = C_{gd} + C_{gs} + C_{para}$. Here, C_{gd} is gate-to-drain capacitance, C_{gs} is gate-to-source capacitance, and C_{para} is parasitic capacitance. The capacitances have been extracted by mixed-mode transient TCAD simulations considering 1 MHz as a default signal frequency. As the temperature increases from 250 K to 350 K, the cut-off frequency of the NC-FinFET decreases by ∼14.6% due to a decrease in the value of the transconductance and total gate capacitance in a moderate to strong inversion regime. However, the impact of transconductance on the unity gain cut-off frequency is more dominant than the total gate capacitance in the super threshold region. Hence, the f_T value of NC-FinFET decreases with the temperature rise. In addition to the f_T, the GBP and TFP are crucial analog/RF performance parameters that need to be addressed for the NC-FinFET for the mm-wave applications. Mathematically given as follows [2, 22]:

$$\text{GBP} = \frac{g_m}{2\pi \cdot 10 \cdot C_{gd}} \tag{8}$$

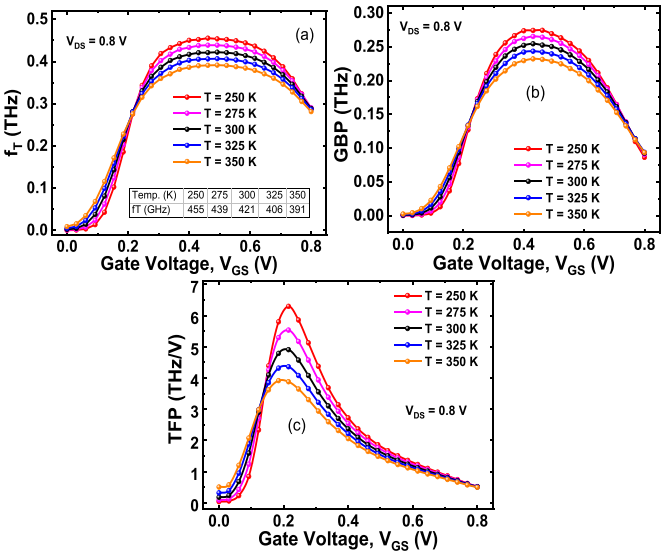

Figure 5. Impact of increasing temperature on (a) f_T (inset: table comprises the extracted peak values of f_T), (b) GBP, and (c) transconductance TFP. Increasing the temperature decreases the g_m, which results in overall decreases in the value of f_T, GBP, and TFP.

$$\text{TFP} = \left(\frac{g_m}{I_D}\right) \cdot f_T. \tag{9}$$

Here, converting 20 dB into ordinary form yields a gain of ten, as a factor taken in equation (8). Figure 5 shows the impact of the rising ambient temperature on the analog/RF merits of the NC-FinFET. As the temperature increases, the carrier mobility decreases, resulting in decreases in g_m value in the moderate to strong inversion region. Thus, the peak value of the unity gain cut-off frequency (f_T), GBP, and TFP starts decreasing with the rising temperature.

Further increase in the gate voltage causes roll-off of the g_m, GBP, and TFP due to mobility degradation caused by the scattering phenomenon. Thus, a proper design guideline is needed for the NC-FinFET to obtain a trade-off between the voltage amplification, intrinsic gain, and analog/RF performance characteristics with the temperature change.

3.4. Impact of temperature on linearity performance of NC-FinFET

The linearity of the modern communication system can be enhanced by subsiding the higher-order coefficients of the transconductance (i.e. g_{m2} and g_{m3}), which ensures that the signal-to-noise ratio improves. The following expression can state the g_{m2} and g_{m3}:

$$g_{m2} = \frac{1}{2!}\frac{\partial^2 I_{DS}}{\partial V_{GS}^2} \tag{10}$$

$$g_{m3} = \frac{1}{3!}\frac{\partial^3 I_{DS}}{\partial V_{GS}^3} \tag{11}$$

where g_{m2} and g_{m3} are defined as the second and third-order derivatives of the drain current. The linearity of the FET-based

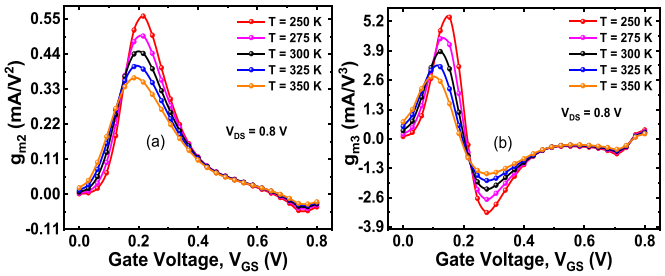

Figure 6. Impact of rising temperature on higher-order transconductance value (a) second-order transconductance (g_{m2}) and (b) third-order transconductance (g_{m3}). As the temperature increases, higher order transconductance g_{m2} and g_{m3} decreases; hence the linearity of the system improves.

system can be enhanced by lowering the peak value of g_{m2} and g_{m3}. Figure 6 shows the impact of rising temperature on g_{m2} and g_{m3}. It can be observed that the peak values of g_{m2} and g_{m3} reduce by raising the temperature from 250 K to 350 K, which shows the salient improvement in the linearity characteristics. At high gate bias (i.e. strong inversion region), g_m decreases (figure 4(a)), resulting in negative values of g_{m2} in the strong inversion region. Thus, singularity is observed for the g_{m3} for those points where g_{m2} is zero. Further, the analog/RF performance merits can be improved for the high-frequency application, provided that the second and third-order VIP_2 and VIP_3 and third-order intercept points (IP_3) should be maximum. This IP_3 can be defined as the point where the input and output power axes (i.e. on logarithmic scales in decibels) cut each other. If it reads from the input axis, it is called IIP_3, and if read by the output axis, it is defined as output IP_3 However, the third-order IMD_3 should be minimum [24]. VIP_2 and VIP_3 is defined as extrapolated gate signal at which the second and third-order harmonics of the signal voltage become equal with the fundament harmonics, given as follows [24, 25]:

$$\mathrm{VIP_2} = 4 \times \left(\frac{g_{m1}}{g_{m2}}\right) \tag{12}$$

$$\mathrm{VIP_3} = \sqrt{24 \times \left(\frac{g_{m1}}{g_{m3}}\right)} \tag{13}$$

Figure 7 shows the effect of temperature on the VIP_2 and VIP_3 characteristics of the NC-FinFET. It can be observed that VIP_2 and VIP_3 are the functions of the temperature, and their peak values modulate while varying the temperature. Increasing the temperature exacerbates the higher-order g_m; thus, the VIP_3 increases, which significantly improves the linearity characteristics. They can be mentioned as:

$$\mathrm{IIP_3} = \frac{2}{3} \times \left(\frac{g_{m1}}{g_{m3} \times R_s}\right) \tag{14}$$

$$\mathrm{IMD_3} = \left[\frac{9}{2} \times (\mathrm{VIP_3})^2 \times g_{m3}\right]^2 \times R_s \tag{15}$$

In our work, we have selected $R_S = 50\ \Omega$, which is a generalized value for analog and RF applications [25]. Figures 8(a)

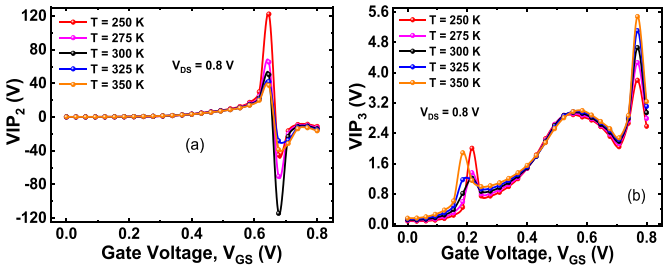

Figure 7. Temperature dependant VIP_2 and VIP_3 of NC-FinFET with varying V_{GS} (a) VIP_2 and (b) VIP_3.

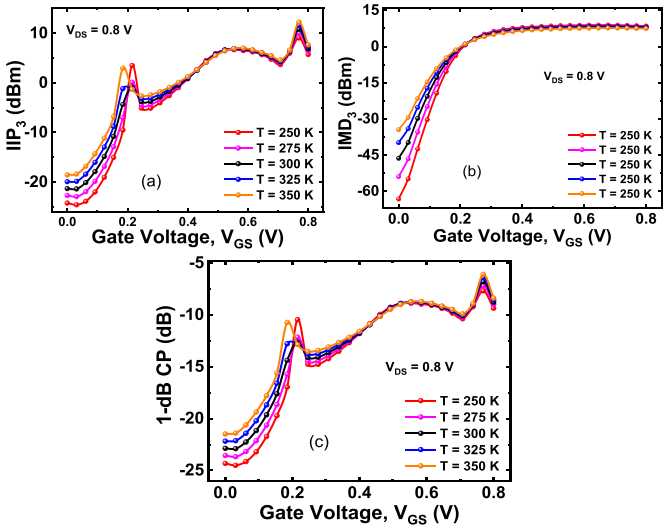

Figure 8. Shows the impact of varying temperature on (a) third-order IIP_3, (b) shows the variation of third-order IMD_3 with varying V_{GS}, and (c) 1 dB CP for the NC-FinFET with applied V_{GS}.

and (b) succinct the effect of temperature on IIP_3 and IMD_3 characteristics of the NC-FinFET. An increase in temperature decreases the third-order transconductance values, which results in decreases in the value of IMD_3 and increases in the values of IIP_3. Thus, the increase in temperature suppresses the distortion. Moreover, it was discerned that at lower gate voltage, the value of IIP_3 is higher than IMD_3 due to suppression of the hot carrier effect at gate dielectric interfaces. Figure 8(c) describes the steady rise of the 1 dB CP for NC-FinFET with the increase in temperature, which is defined as:

$$1\ \mathrm{dB\,CP} = 0.22 \times \sqrt{\frac{g_{m1}}{g_{m2}}} \tag{16}$$

The 1 dB CP for NC-FinFET improves with an increase in temperature for the moderate to strong inversion region. Hence, the linearity merits of NC-FinFET would be enhanced with temperature.

3.5. Impact of temperature on NC-FinFET-based common source amplifier and ring oscillator

We have thoroughly analyzed the impact of temperature on the frequency compatibility of the designed NC-FinFET

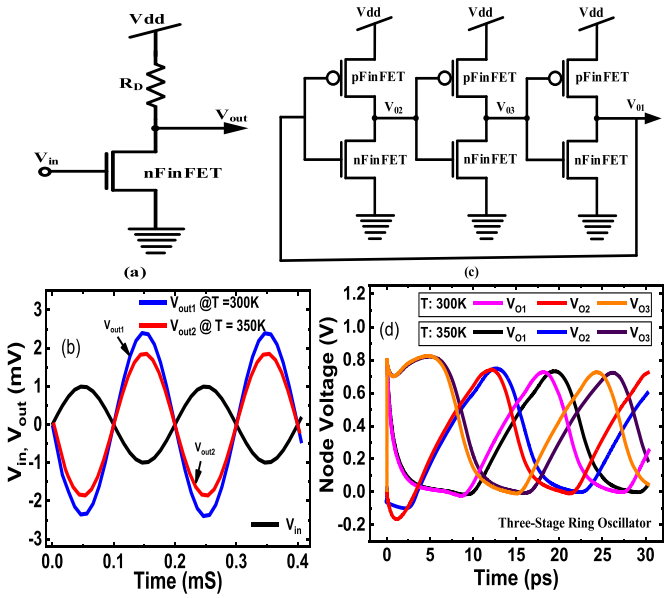

Figure 9. Analysis of single-stage CS amplifier and three-RO circuit using mixed-mode simulation. (a) Schematic diagram of the CS amplifier with the chosen resistive load (R_D). (b) Transient analysis of the applied sinusoidal signal (V_{int}) and output signal (V_{out}) across the CS amplifier and shows that the voltage gain of the CS amplifier decreases while increasing the temperature from 300 K to 350 K, (c) schematic of a three-stage RO, made up of *p*-type, and *n*-type NC-FinFET connected in back-to-back fashion; (d) shows the sustained output waveform of a three-stage RO.

through the designed single-stage CS amplifier with the resistive load (R_D) (figure 9(a)) and three- RO (figure 9(c)) circuit using the transient analysis. A two-level Newton-Rapson coupled algorithm is invoked to solve the interdependence device and circuit co-simulation matrices [17]. TCAD mixed-mode framework solves different semiconductor equations to evaluate the requisite device matrices, and different circuit matrices are evaluated by solving the self-contained circuit parameters.

The intrinsic gain is the ratio of transconductance (g_m) and output conductance (g_{ds}). The voltage gain (A_V) of the *n*-type NC-FinFET single stage CS amplifier possessing resistive load (R_D) is given as [26]:

$$A_V = \frac{V_{out}}{V_{in}} = -g_m \times (r_o \parallel R_D) \simeq -g_m R_D \qquad (17)$$

where r_o is the output resistance, and at the quiescent point, the r_o is very large ($r_o \simeq \infty$), which shows that the variation in the output voltage (V_{out}) is dominated by the transconductance (g_m), and the gain is severely affected by the rising temperature variation.

Figure 9(b) shows the variation of the output waveform (V_{out}) while varying the input waveform (V_{in}) at temperatures 300 K and 350 K. As the temperature increases, the transconductance decreases, which decreases the voltage gain of a single-stage CS amplifier. Hence the peak amplitude of the output waveform decreases. For the analysis of RO, we have created a *p*-type FinFET and calibrated it with the same experimental data [3]. Then, we connected the *p*-type FinFET and *n*-type FinFET to form an inverter as a stage of the ring oscillator using mixed-mode simulations. The RO provides a sustained oscillation at the output. The sustained oscillation frequency and single inverter delay are observed as 95.78 GHz (86.30 GHz) and 1.74 ps (1.93 ps) at 300 K (350 K), respectively.

4. Conclusion

This paper thoroughly investigated the effect of varying temperature on the linearity and analog/RF performances of NC-FinFET. The temperature significantly impacted the intrinsic characteristics of the BL FinFET through carrier mobility and bandgap. Furthermore, extrinsically, the Landau parameters of the FE layer are strongly dependent on temperature (especially α). Thus, the overall impact of temperature on device's analog/RF merits, such as gate capacitance, intrinsic gain, transconductance, etc, has been investigated. Similarly, the linearity characteristics, such as g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3, etc, have been investigated with varying temperatures from 250 K to 350 K. The results reveal that analog/RF merits have deteriorated, whereas linearity merits have been improved with increasing temperature. Moreover, we designed a CS amplifier and three-RO using mixed-mode simulation and investigated the impact of temperature on the output waveforms. Thus, the suitable guidelines are worth needed to design a reliable NC-FinFET under varying temperature conditions.

Data availability statement

The data generated and/or analysed during the current study are not publicly available for legal/ethical reasons but are available from the corresponding author on reasonable request.

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