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Insights into the operation of negative capacitance FinFET for low power logic applications

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ABSTRACT

In the incessant search to overcome the power densities and energy efficient limitations, performance matrix of emerging electronic devices are being explored inevitably to find the alternatives of MOSFETs. We investigated and compared the delay and energy performance matrices of fin-shaped FET and negative capacitance FinFET (NC-FinFET) based devices and circuits designed on the same technology node. The improvement in the performance of NC-FinFET based CMOS circuits is enhanced due to the negative capacitance's negative DIBL by employing a industry standard BSIM-CMG model. After analyzing at the device-level, detailed evaluation is carried out at logic level for embedded inverter chain, three-stage ring oscillators (ROs), and 2-bit ripple carry adders (RCA) for frequencies ranging between 10 kHz–1 GHz. Our findings revealed that the NC-FinFET based circuit has a lower delay for a given range of operating frequencies and saves a significant amount of power when compared to baseline FinFET, making NC-FinFET desirable for low power digital logic applications.

1. Introduction

In the recent years, FinFET-based logic devices are attaining more popularity due to their low standby power dissipation, better scalability, high electrostatics channel control, improved subthreshold swing (SS), and high-performance compared to the conventional bulk MOSFET [1]. The FinFET-based logic devices and circuits are already in volume production to satisfy the impeccable need for high speed wireless network, mobile computing system, and implantable medical devices (IMDs) which require low power circuits [2]. FinFETs based transistors have the advantage due to their thin body structure and better channel control from the surrounding sides. The FinFET scaling from 22- to 7-nm technology node has been successfully achieved [3,4]. Further scaling of FinFET below 3-nm technology node is arduous due to its intrinsic architecture. Apparently fin pitch of 24 nm and fin height of 60 nm has been reached to its saturation limit of scaling and further making thinner and taller fins is not possible due to etching and cleaning issues arising during manufacturing. Nowadays, negative capacitance field-effect-transistors (NCFETs) are promising suitable candidates for the development of sub-3-nm technology node CMOS devices and circuits due to their outstanding performance and high manufacturing process compatibility with the existing CMOS technology [5–10]. The NCFETs-based device consists of a ferroelectric (FE) material in the gate stack of a baseline FET; as a result, the internal voltage of the baseline transistor is amplified by the FE-layer, resulting in a significant improvement in the I_{ON}/I_{OFF} ratio as well as an improvement in the sub-threshold slope (SS). Because of this V_{DD} scaling, NCFETs have the potential to overcome the Boltzmann tyranny, which limits the SS (60 mV/decade) at room temperature (300 K) [11]. For designing of energy efficient circuit for low power applications the scaling of device dimension is a critical parameter however the scaling of V_{DD} is limited to threshold voltage (V_{TH}) operation regions. Further scaling of V_{DD} beyond the V_{TH} limit will result in energy degradation and speed loss of CMOS based circuits [12]. Negative capacitance based FETs device have the advantage to operate at lower supply voltage and exhibiting higher ON-state current and steep switching characteristic (i.e. SS < 60 mV/decade at 300 K) compared to the standard MOSFET [13–15]. Hence, at high frequency, NCFETs based circuits such as comparator [16,17], differential amplifier [18], current

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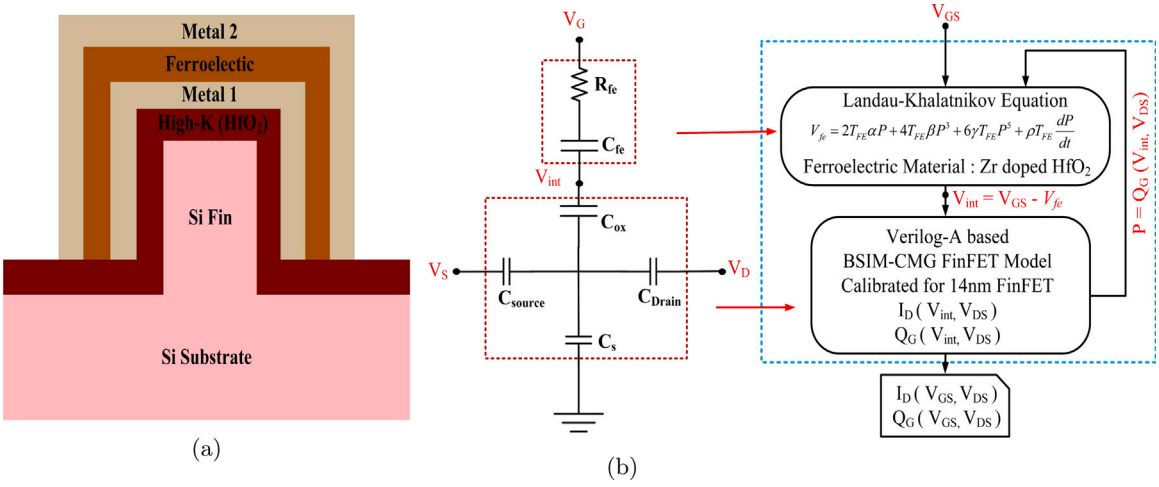


Fig. 1. (a) Cross sectional view of Negative Capacitance FinFET (b) Equivalent capacitance circuit representation: The positive capacitance of the intrinsic FinFET stabilized the negative capacitance of the ferroelectric layer and Self-consistent based compact modeling approach of the NC-FinFET by using the BSIM-CMG. Flow chart adopted to capture the impact of V_{FE} in terms of V_{int} and ultimately V_{GS}.

mirrors [18,16,19,20], analog switches [18,19], and sample-and-hold circuits [11] have clocked for better performance compared with that conventional FETs based device, while keeping V_{DD} constant . The ON-state current gain is accompanied by the presence of FE material in the gate stack which results in increase in the gate capacitance. However the presence of non-linear ferroelectric capacitance with other capacitance present in the device and circuit needs to be evaluated to get insight into the overall benefit of NCFETs at the circuit level and avert any deleterious effect [21–24]. In this paper, we have evaluated the delay and energy performance of NC-FinFET based logic circuits by analyzing the effect of ferroelectric thickness (T_{FE}), negative drain induced barrier lowering (NDIBL) and negative differential resistance (NDR) on the NC-FinFET device. These parameters are very crucial for the circuit design and need to be properly investigated to find out the optimized T_{FE}. Further, the effect of above parameters are intensively analyzed to get insights into the circuit performance. The organization of this paper is as follows: In Section 2, basics of NC-FinFET, its modeling methodology and device level analysis of NC-FinFET are discussed. In Section 3, we have analyzed the static and dynamic performance of a NC-FinFET based CMOS inverter. Section 4, evaluate the delay and energy performance in NC-FinFET based embedded inverter chain, ring oscillator and RCA, followed by conclusion (Section 5) in the end.

2. NCFinFET: Design & analysis

This section discusses the basics theory, modeling framework and device level analysis needed for the investigation of NCFinFET in logic applications.

2.1. NCFinFET: Basics

The cross sectional view of NC-FinFET and its equivalent voltage divider capacitance circuit is shown in Fig. 1. The device contains a ferroelectric (FE) layer in the gate stack and internal metal layer is used to create an equipotential surface V_{int}. Due to this arrangement the baseline FinFET and ferroelectric (FE) can be treated as two different structures connected by a wire will greatly simplify the compact modeling of the proposed NC-FinFET structure [25,26]. Hence, the requisite properties of NC-FinFET is obtained by interactions of the positive capacitance of the baseline FinFET with the negative capacitance of the FE layer. This distinctive property of negative capacitance appears due to the unique relation between the polarization (P) and electric field (E) of the FE material [5,27], which can be modeled by the following expressions:

$$E_{fe} = \frac{V_{fe}}{T_{FE}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho\frac{dP}{dt}. \quad (1)$$

Here, α, β and γ are the static and material specific Landau parameters coefficients. The value of α is temperature sensitive whereas β and γ are temperature independent parameters for a given FE material. In the above equation it is assumed that the polarization profile is uniform due to the homogeneous monodomain of FE material [28,29]. ρ is the ferroelectric damping constant which relates polarization response of FE material with the applied electric field. A FE material having low value of damping constant ($\rho < 0.1\ \Omega m$) is required for design of faster switching characteristics CMOS circuits than the baseline FinFET [30]. Because large value of ρ slows down the transient switching characteristics even if FE material is competent to provide internal voltage amplification [31]. So, the low value of ρ was selected as mentioned in [7,32] to analyze the delay of the NC-FinFET based logic devices in this paper. Furthermore, ρdP/dt becomes negligible for a quasi-static analysis. Then the approximate value of electric field can be given as

$$E_{fe} \approx 2\alpha P + 4\beta P^3. \quad (2)$$

The FE static coefficient α and β can be related in terms of remnant polarization P_r and coercive field E_c as

$$\alpha = -\frac{3\sqrt{3}}{4}\frac{E_c}{P_r} \text{ and } \beta = \frac{3\sqrt{3}}{8}\frac{E_c}{P_r^3}. \quad (3)$$

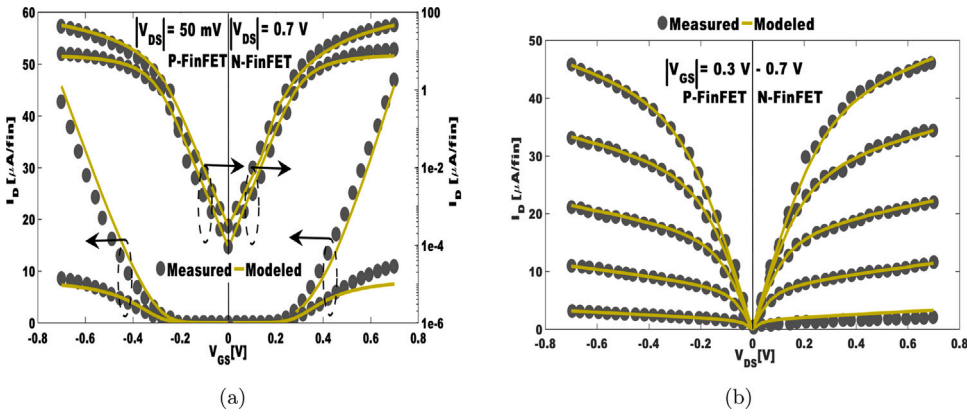
The ferroelectric capacitance C_{fe} can be obtained as $C_{fe} = dP/dV_{fe}$, where $V_{fe} = E_{fe} * T_{FE}$ and T_{FE} represents the voltage drop and thickness of the FE material, respectively. Mathematically

$$C_{fe} \approx \frac{-3.84 * P_r(\mu C/cm^2)}{T_{FE}(nm) * E_c(MV/cm)}\ \mu F/cm^2 \text{ for } |\alpha| \gg 6\beta P^2. \quad (4)$$

The oxide capacitance (C_{ox}) of baseline transistor is given as

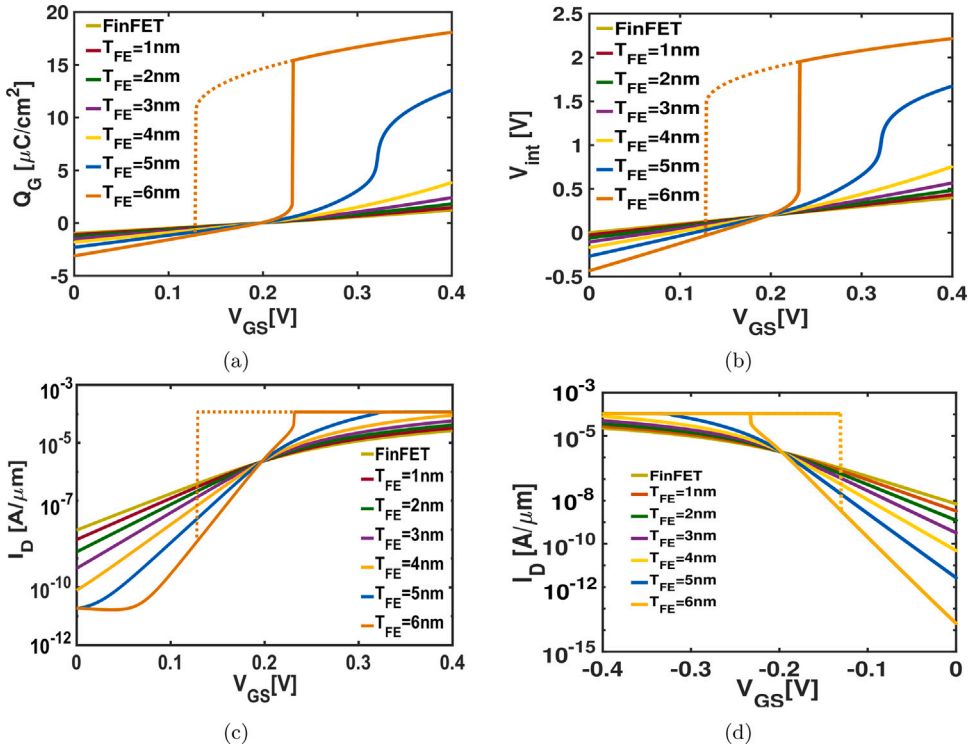
$$C_{ox} = \frac{\epsilon_{ox}}{T_{ox}} = \frac{\epsilon_{SiO_2}}{EOT} \approx \frac{3.45}{EOT(nm)}\ \mu F/cm^2 \quad (5)$$

where ϵ_{ox} and ϵ_{SiO_2} represent the permittivity of high-k and SiO_2, respectively. T_{ox} represents the physical thickness of high-k dielectric. The unique properties of ferroelectric material in the NC-FinFET is obtained by the interactions of negative and positive capacitance of the FE layer with the baseline transistor, respectively. Fig. 1(b) can be used to understand the capacitive interactions of NC-FinFET devices. $\rho\frac{dP}{dt}$ in Eq. (1) can be modeled as $R_{fe}(\rho\frac{T_{FE}}{A_{FE}})$ as explained in [21]. Here



(a) (b)

Fig. 2. Calibration of the baseline 14 nm HP technology node n-FinFET and p-FinFET (a) Transfer characteristics ($I_D - V_{GS}$) and (b) output characteristics ($I_D - V_{DS}$) with the experimental result in [33] for the extraction of the requisite parameters in the simulation work.



(a) (b) (c) (d)

Fig. 3. (a) Illustration of variation in gate charge by varying the gate voltage in a n-type NC-FinFET at different value of T_{FE}, (b) Impact in internal voltage by varying the gate voltage in a n-type NC-FinFET at different value of T_{FE}, $I_D - V_{GS}$ characteristics of (c) n-type-NC-FinFET, and (d) p-type-NC-FinFET for different value of T_{FE} at $|V_{DS}|$ = 0.4 V. The OFF current of NC-FinFET reduces for higher values of V_{DS}.

A_{FE} is the cross-section area of the FE layer and it is equivalent to the cross section area of baseline intrinsic FinFET. Here, V_S, V_G, and V_D represent the voltage applied across the source, gate and drain of the NC-FinFET, respectively. V_{int} the voltage present across the interface of FE material and dielectric of the baseline transistor (also referred as the internal gate of the baseline transistor). C_{ox} is the positive gate capacitance of the baseline transistor. The effective gate capacitance (C_{Gfe}) of NC-FinFET can be obtained by putting the value of α, C_{fe} and C_{ox} from Eqs. (3)–(5), respectively. Mathematically,

$$C_{Gfe} = \frac{|C_{fe}|.C_{ox}}{|C_{fe}| - C_{ox}} = \frac{3.45}{EOT(\text{nm}) - 0.7|\alpha|(\text{cm/pF}) * T_{FE}(\text{nm})}\ \mu\text{F/cm}^2 \quad (6)$$

The condition for $C_{Gfe} > 0$ requires the thickness of FE material should be less than the critical thickness (T_c) to obtain the hysteresis free operation given as follow:

$$T_{FE} \leq \frac{1.44EOT(\text{nm})}{|\alpha|(\text{cm/pF})} \equiv T_c\ (\text{in nm}) \quad (7)$$

According to above equation, for a given ferroelectric material, increasing the (T_{FE}) will increases the capacitance (C_{Gfe}) of the device. Increasing the (C_{Gfe}) will have impact on the propagation delay of the logic device made from NCFinFET and it need to be evaluated which is the scope of this paper.

2.2. Modeling and simulation framework

The analysis in this paper is based on solving the self-consistent time-dependent single domain Landau–Khalatnikov (L–K) equation with the baseline transistors equations in the SPICE [34]. By solving the self-consistent equation the device currents, internal gate voltage (V_{int}), and ferroelectric polarization can be obtained in terms of

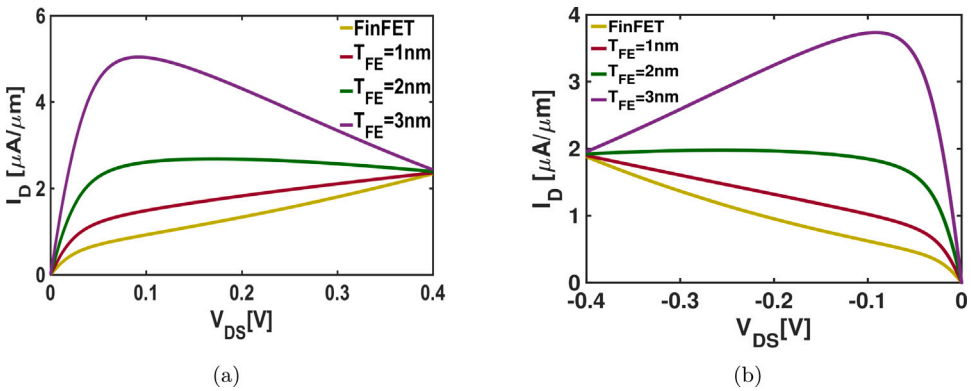


Fig. 4. $I_D - V_{DS}$ characteristics of NC-FinFET for different value of T_{FE} by varying the drain voltage (a) at $V_{GS} = 0.2$ V for n-NC-FinFET, and (b) at $V_{GS} = -0.2$ V for p-NC-FinFET. NC-FinFET show NDR at $T_{FE} = 3$ nm, which limits the non-hysteresis operation of NC-FinFET based circuit.

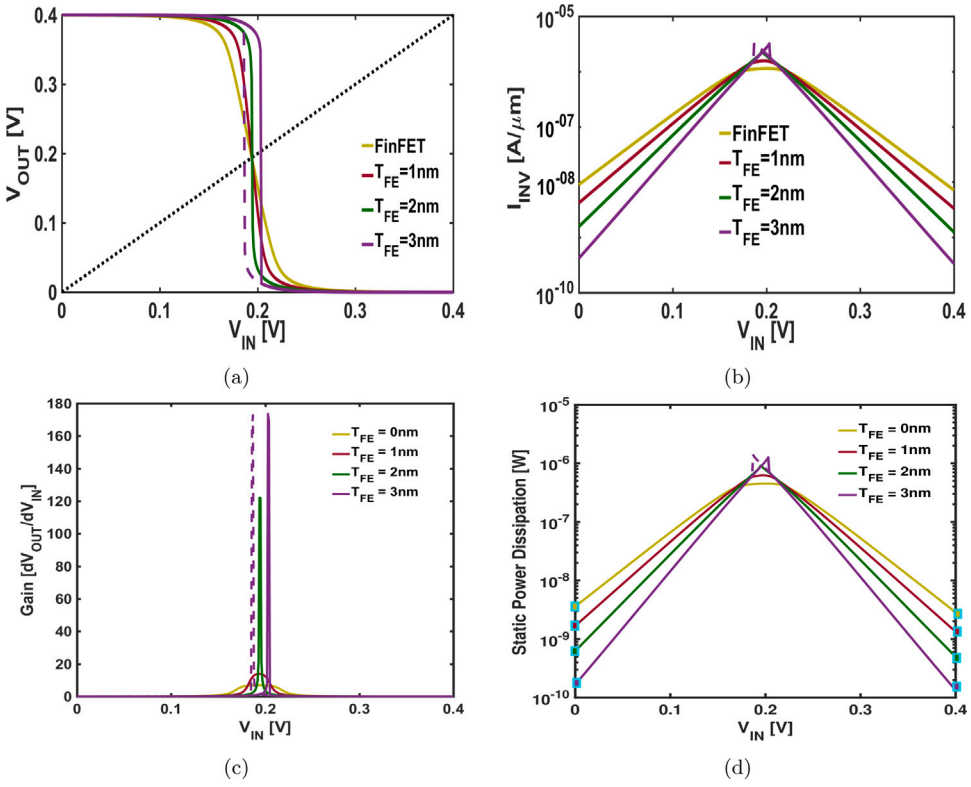


Fig. 5. (a) Voltage Transfer Characteristics, (b) Inverter current (c) Inverter gain (d) Static power dissipation of the baseline FinFET and NC-FinFET inverter at different values of T_{FE}, which improves as T_{FE} increases.

gate/drain/source applied voltages. The working methodology of the self-consistent method used in this work is depicted in Fig. 1 (b). The gate charge density (Q_G) of well calibrated 14 nm HP baseline FinFET extracted from the BSIM-CMG compact model is provided into the L–K model, which produces the voltage drop across the ferroelectric (V_{fe}). The resultant voltage is used to calculate the internal voltage ($V_{int} = V_{GS} - V_{fe}$), where V_{GS} is the applied gate voltage. Finally, the V_{int} voltage is fed back into the input of the BSIM-CMG model. We have used MFMIS structure to improve the performance by balancing the nonuniform potential at the ferroelectric dielectric interface [14]. Also, MFMIS structure is experimentally demonstrated [35] and excels high ON current and incurs a hysteresis at a larger ferroelectric thickness than the NC-FinFET without metal 1 [36]. Reference baseline transistors have gate, source, drain and substrate as electrodes however the V_{int} is introduced as a virtue of SPICE based implementation obtained as a function of V_{DS} and V_{GS}. The baseline transistor has been modeled by employing the 14 nm HP predictive technology model card to the well known industry standard BSIM-CMG model by properly incorporating the short channel effect [34,37]. BSIM-CMG compact model written in Verilog-A language for the baseline FinFET is numerically very robust and efficient and suitable for large logic and circuit simulations like ours. The various device parameters extracted from the experimental data in [33] are used in the simulation are well calibrated for the baseline FinFET [Fig. 2] using the BSIM-CMG compact model by extracting the SS, DIBL, velocity saturation, series resistance, mobility degradation, etc. in the 14 nm HP predictive technology model card. These device parameters incorporated are: Channel length (L_g= 18 nm), Fin height (F_h= 50 nm), Fin width (F_w= 12 nm), Equivalent oxide thickness (T_{EOT}= 0.75 nm), and work function of Metal 1 and Metal 2 have been selected as 4.41 eV for n-type FinFET and 4.75 eV for p-type FinFET, respectively.

Table 1 describes requisite FE material (zirconium doped HfO_2) parameters and their corresponding nominal value used in our simulation.

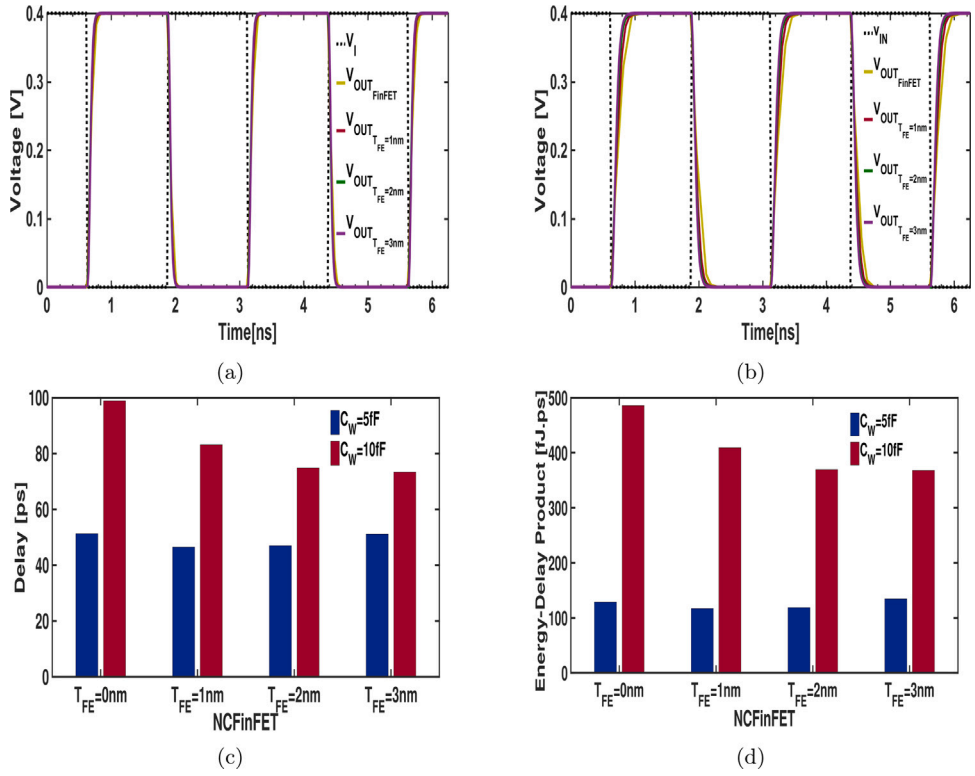


Fig. 6. Input–Output Transient Characteristics of an inverter for (a) C_L = 5 fF and, (b) C_L = 10 fF (c) Delay and, (d) Energy-Delay Product at 400 MHz frequency.

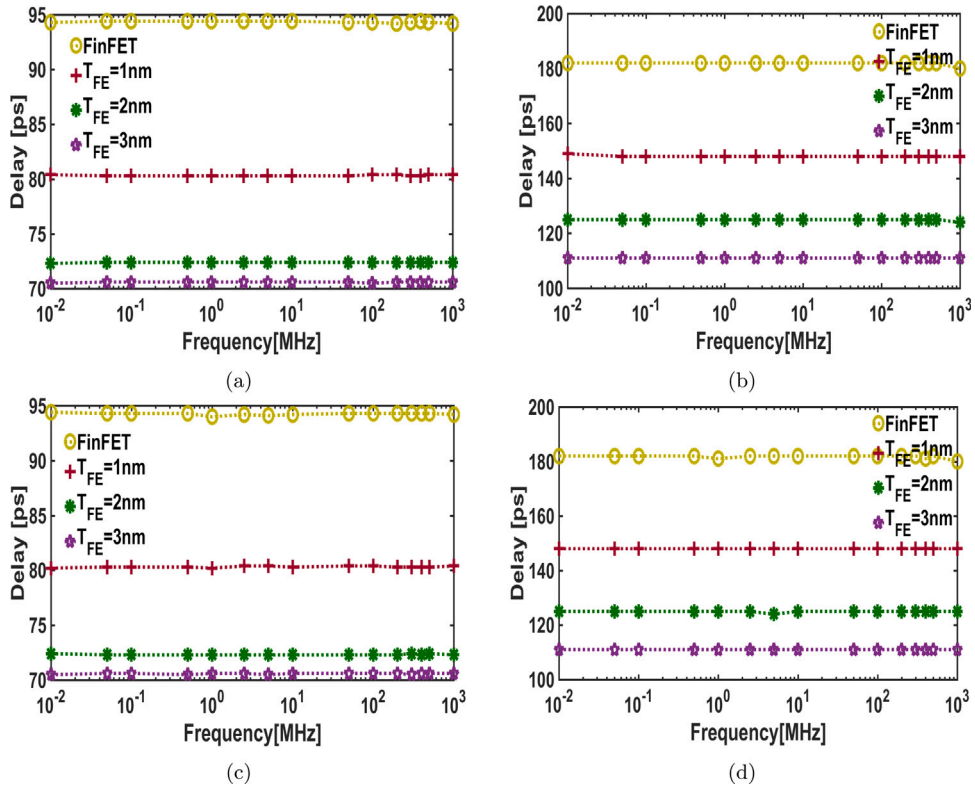


Fig. 7. Delay analysis of n-stage negative capacitance embedded inverter circuit for mid frequency range (a) inverter-5 at C_W = 5 fF, (b) inverter-5 at C_W = 10 fF (c) inverter-6 at C_W = 5 fF and (d) inverter-6 at C_W = 10 fF.

The values of α, β and γ are extracted from the experimental data of the P–E hysteresis curve [38,39]. FE material having non-zero and negative value of γ will have non-physical FE properties exists for large $|P|$. So, the desired characteristics of ferroelectric can be obtained in negative capacitance region by proper selecting the value of $|P|$. In our analysis we have selected the value of polarization between the - 20

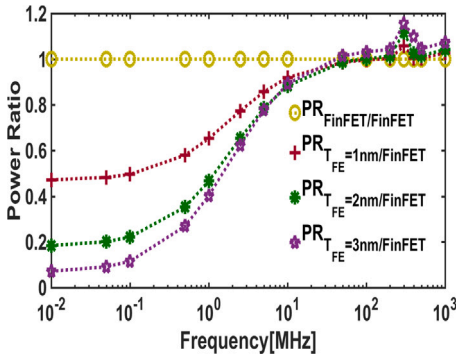


Fig. 8. Power ratio versus frequency for INV-5 in embedded inverter chain at C_W = 10 fF.

Table 1
Simulation parameters for NC-FinFET.

Parameters	Values	Unit
α	-1.17×10^9	m/F
β	4.9×10^9	$m^5/F/C^2$
γ	-3.9×10^9	$m^9/F/C^4$
ρ	0.05	Ωm

μC/cm^2 and 20 μC/cm^2 (negative capacitance region) for non-physical characteristics even for a negative γ value.

2.3. NCFinFET: Device analysis

We begin with discussing the impact of T_{FE} on the various device characteristics so that it can provide the base for the analysis of the NC-FinFET based logic circuits. Due to stacking of ferroelectric material in the gate the V_{int} voltage is amplified due to the intrinsic properties of ferroelectric material [Fig. 3(b)] which results in the charge enhancement [Fig. 3(a)] and leads to the high drive current for the inverter [Fig. 5(b)]. Fig. 3(c) and (d) describe the transfer characteristics ($I_D - V_{GS}$) of the n-type NC-FinFET and p-type NC-FinFET, respectively. Work function tuning of metal is used to match the threshold voltage for the n-type NC-FinFET and p-type NC-FinFET. The $I_D - V_{GS}$ characteristics become steeper with the increase in the value of T_{FE} due the voltage amplification provided by the FE layer stacked in the gate. However, as we increase the value of V_{DS} the value of I_{OFF} decreases as compared to baseline FinFET transistors, this result is due to the dependence of V_{int} with the V_{DS} apart from V_{GS}. This is because the value of polarization decreases when the drain voltage V_{DS} increases. Further increase in the value of T_{FE} decreases the ferroelectric capacitance as compared to the drain coupling factor which yields a larger reduction in the value of I_{OFF} [40]. At a low value of V_{DS} this effect is negligible and the I_{OFF} current has similar performance as compared to baseline FinFET. Intuitively, higher V_{DS} has two different effects on the drain current. At higher applied electric fields the drain current (I_{ON}) increases due to dominance of ferroelectric capacitance as compared to drain coupling factor. However, at lower electric fields due to dominance of drain coupling factor a reverse impact on the V_{int} will be created, hence the value of the drain current (I_{OFF}) decreases. These two opposite effects of V_{DS} on the drain current are known as the negative drain induced barrier lowering (NDIBL) as shown in Fig. 3(c) and (d). At a larger value of T_{FE} the value of OFF current decreases due to dominance of V_{DS}. The comprehensive details of I_{ON}, I_{OFF}, and SS of the n-type NC-FinFET at different T_{FE} is shown in Table 2. The effect of V_{DS} on the performance of drain current is also depicted on the output characteristics [Fig. 4]. However, $I_D - V_{DS}$ characteristics have also dependency on the V_{GS}, T_{FE}, and characteristics of the baseline FinFET apart from V_{DS} [16]. At lower ferroelectric thickness (T_{FE}= 1 nm and 2 nm) the $I_D - V_{DS}$ characteristics is similar to that of the baseline FinFET with larger ON current, which is due to the dominance of ferroelectric capacitance over drain coupling factor. However, as the T_{FE} increases the ferroelectric capacitance decreases and becomes comparable to drain coupling factor so the relative values of V_{DS} and V_{GS} will control V_{int}, and V_{int} decreases with an increase in V_{DS}, Hence, the drain current decreases as the value of V_{DS} increases, thus the output characteristic exhibits negative differential resistance (NDR). So, $I_D - V_{DS}$ characteristics start showing NDR at T_{FE}= 3 nm which limits the operation of NC-FinFET based circuits.

3. NC-FinFET inverter: Static & Dynamic analysis

Fig. 5(a) illustrates the VTC of the FinFET and NC-FinFET based inverter at different T_{FE}. Gate stacking of ferroelectric material provides the voltage amplification due to this the gain in the transition regions increases [Fig. 5(c)] means the VTCs become sharper as compared to VTC's of the baseline FinFET. As the curve becomes sharper while increasing the T_{FE} the noise margin also enhances.

A contradictory behavior is observed in Fig. 5(a) at T_{FE}= 3 nm that the NC-FinFET's VTC is showing the hysteresis in the transition region although the corresponding device is exhibiting the non-hysteresis behavior. This peculiar behavior is attributed to the NDR observed in the output characteristic [Fig. 3(c)]. Table 3 shows the DC static performance parameter of baseline FinFET and NC-FinFET for different values of T_{FE} obtained for non-hysteresis operation. NDIBL decreases the leakage current of the inverter [Fig. 5(b)] which results in improvement of static power dissipation [Fig. 5(d)] and Noise Margin with increasing T_{FE}. At T_{FE}= 3 nm, NC-FinFET based inverter will exhibit 95.50% power saving compared to baseline FinFET based inverter. Fig. 6(a), (b) shows the transient response of the NC-FinFET based inverter at different load capacitance. The delay of the NC-FinFET based inverter circuit has dependency on the load capacitance (C_W). The delay of the inverter circuit increases as the value of the C_L increases [Fig. 6(b)]. Fig. 6(c), (d) compares the delay and energy-delay product of inverter obtained at 400 MHz frequency for different load capacitance. It can be observed that with increasing thickness, delay of the inverter decreases and significant improvement in the energy-delay product at 400 MHz input frequency is obtained.

4. NC-FINFET logic circuits: Case studies

This section deals with performing transient analysis to understand the circuit's perspective of NCFinFET based logic devices. Although, by performing DC analysis of the NC-FinFET inverter in Section 3, unconventional NDR effect can be observed in the VTCs curve. The hysteresis characteristics observed can be utilized in the designing of memory applications like static random access memories (SRAM). The purpose of performing the transient analysis is to understand the energy-delay simulation characteristics of the NC-FinFETs based logic circuits for which we have analyzed the three case studies: embedded inverter chain, 3-stage ROs and 2 bit Ripple Carry Adder (RCA).

4.1. Embedded inverter chain

Eleven-stage inverter chain is analyzed with different input switching frequencies ranging from 10 kHz to 1 GHz to study the trends of energy and delay at different NC thickness. To get the practical scenario we have analyzed INV-5 and INV-6 in the inverter chain for delay and energy calculation at two different load capacitance C_W= 5 fF and C_W= 10 fF. As shown in Fig. 7 faster operation or delay reduction is obtained as we increases the thickness of the NC in comparison to baseline FinFET. This happens because delay of the NCFinFET inversely depends on the driving strength of the NCFinFET, ρ of the FE material, and wire capacitance. With increasing NC thickness driving strength of NCFET increases which leads to the reduction of delay. Also, the

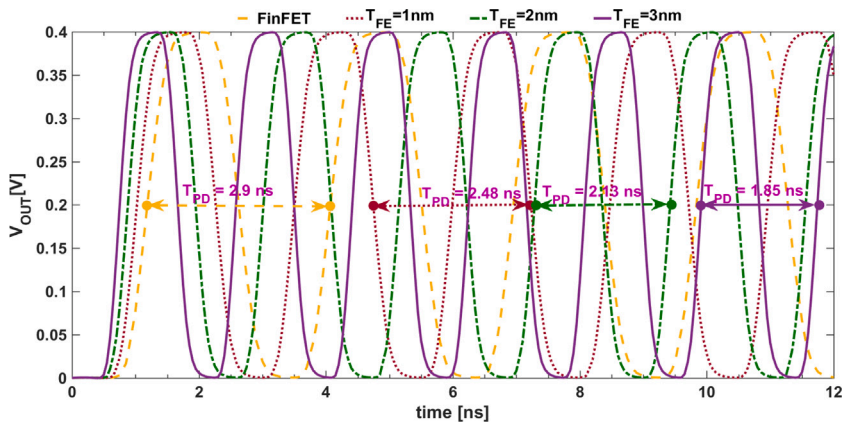


Fig. 9. Demonstration of input–output transient characteristics of the NC-FinFET based ROs at different vale of T_{FE}. The delay performance of the ROs improves as the value of T_{FE} increases.

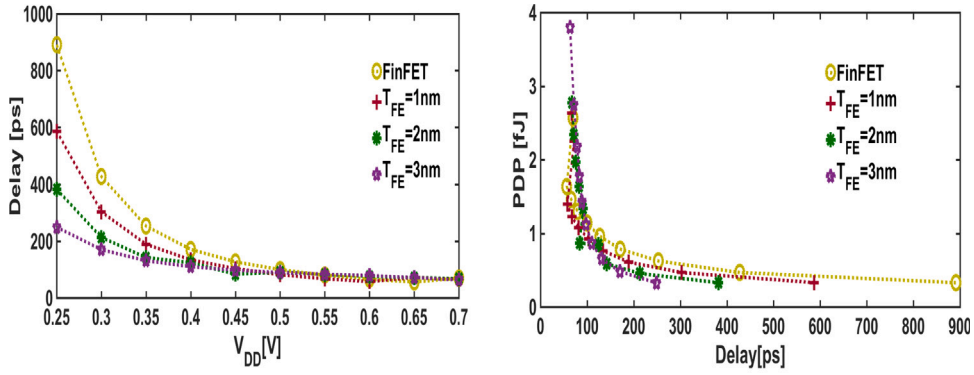


Fig. 10. (a) Delay-V_{DD} plot elucidating the decrease in delay with respect to V_{DD} for lower value of V_{DD}. (b) Energy-Delay simulation curve demonstrating reduction in energy of an inverter stage in the three-stage RO circuits for different values of T_{FE} at C_W = 10 fF.

Table 2
n-type NC-FinFET device performance parameters at different value of T_{FE} and $V_{GS} = V_{DS} = 0.4$ V.

Parameters	FinFET	NC-FinFET (T_{FE} = 1 nm)	NC-FinFET (T_{FE} = 2 nm)	NC-FinFET (T_{FE} = 3 nm)	NC-FinFET (T_{FE} = 4 nm)	NC-FinFET (T_{FE} = 5 nm)
I_{ON} (μA/μm)	26	31.7	40.6	56.3	88.1	115
I_{OFF} (nA/μm)	9.38	4.4	1.65	0.647	0.0782	0.018
SS_{avg} (mV/dec.)	79.03	69.97	61.09	51.81	42.73	33.69

Table 3
Static Performance Parameters for NC-FinFET based Inverter.

Parameters	FinFET	NC-FinFET (T_{FE} = 1 nm)	NC-FinFET (T_{FE} = 2 nm)	NC-FinFET (T_{FE} = 3 nm)
$NoiseMargin_H$ (mV)	170	182	194	204
$NoiseMargin_L$ (mV)	157	170	183	195
$I_{OFF,p}$ (nA)	8.97	4.19	1.56	0.419
$I_{OFF,n}$ (nA)	7.13	3.33	1.24	0.335
$StaticPowerDissipation_p$ (nW)	3.588	1.676	0.624	0.1676
$StaticPowerDissipation_n$ (nW)	2.852	1.332	0.496	0.134

Table 4
Energy Delay Metrics for RCA @ 100 MHz.

Parameters	FinFET	NC-FinFET (T_{FE} = 1 nm)	NC-FinFET (T_{FE} = 2 nm)	NC-FinFET (T_{FE} = 3 nm)
$Delay$ (ns)	0.626	0.494	0.403	0.351
$Energy$ (pJ)	0.143	0.141	0.142	0.151
EDP (pJ · μs)	89.52	69.65	57.22	53

delay of the embedded inverter have a significant impact of varying the load capacitor C_W. The delay of the embedded inverter increases while increasing the value of C_W [Fig. 7(a), (b)]. Fig. 8 shows the power ratios versus mid band input switching frequency which varies from 10 kHz to 1 GHz means input changes from 100 μs to 1 ns for INV-5. The figure elucidates the baseline FinFET power and NC-FinFET power for different values of T_{FE}. These results were obtained for consecutive frequencies by varying the clock cycle and accommodating the delays and other non-idealities. Symbols in the curve lower than 1 indicate that the NC-FinFET power is lower as compared to the baseline FinFET

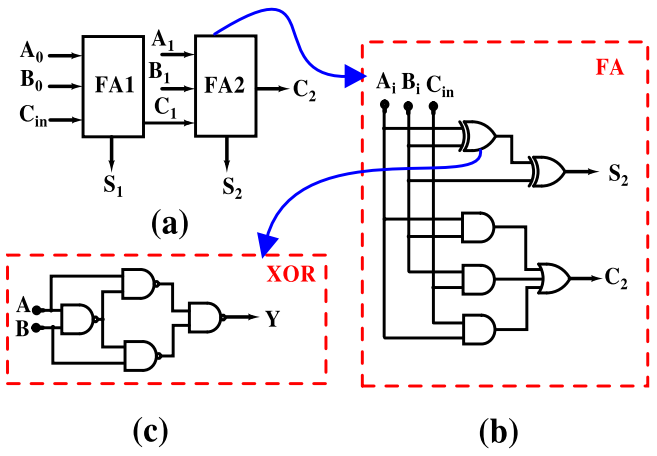


Fig. 11. (a) Schematic Diagram of the 2 bit Ripple carry adder.(b) Equivalent Circuit diagram of Full adder composite of NAND gates. (c) XOR circuit representation in terms of NAND gates.

power. Means, these symbols will describe the power advantage for the NC-FinFET circuits as compared to the baseline FinFET. Values larger than 1 describe that the NC-FinFET power is higher than the corresponding baseline FinFET power meaning the power loss will occur for these operating frequencies. So NC-FinFET is showing improved power ratio for lower frequencies and slightly degrades at gigahertz frequencies. This happens because ferroelectric crystal material must be able to switch between the polarization states in order to obtain the power efficient embedded inverter chain. FE materials have two stable states, however at gigahertz frequency electric field changes too quickly due to this the polarization is trapped between one of its stable states and the ferroelectric capacitor will not exhibit voltage amplification which will hamper the negative capacitance phenomenon. In that scenario the circuit's will exhibit the power loss at gigahertz frequency. This power loss is also experimentally verified [41,42]. So it is worth concluding that the insertion of FE material at gigahertz frequencies can lead to voltage attenuation.

4.2. Ring oscillator

To analyze the energy delay benchmarking we studied the behavior of NC-FinFET in three-stage inverter-based ring Oscillators (ROs). Fig. 9 shows the input–output transient curve at V_{DD} = 0.4 V and C_L= 10 fF, which elucidates that increasing the thickness of ferroelectric decreases the delay in the ROs compared to baseline FinFET. As shown in Fig. 10 it can be observed that NC-FinFET based ROs show reduction in delay for V_{DD} < 0.45 V. For V_{DD} > 0.45 V this matrices have no significant effect of ferroelectric phenomenon and also slightly degrade with respect to baseline FinFET transistors. In addition to this, the energy-delay diagram [Fig. 10(b)] show a intersection point.

These trends are associated with the material's ferroelectric damping constant parameter ρ. For higher V_{DD} > 0.45 V, due to ρ the R_{FE} term discussed in Section 2 become significant and effect the delay performance of the NC-FinFET based ROs. Reduction in R_{FE} is desired for enhanced benefits of the NC-FinFET for a larger range of V_{DD}. Therefore, ferroelectric material having low value of ρ and NC-FinFET device showing non-hysteresis steep switching is required to minimize the ferroelectric polarization lag with respect to the electric field.

4.3. Ripple carry adder

To evaluate NC-FinFET performance for logic devices we have analyzed a 2 bit RCA and evaluated it for baseline FinFET and NC-FinFET for different values of T_{FE}. The corresponding equivalent circuit and its composite elements are shown in Fig. 11. The full adder circuit is designed by using the 2-input NAND gates and 3-input NAND gates. The gate size and parasitic capacitance are equally selected for both the RCA. The delay and energy of the RCA circuit is evaluated by using a clock having a variable input transition. Input data set of A (11) is fixed and B input data set is switched between (11) and (00). Table 4 shows the requisite result obtained at 100 MHz frequency. Delay and energy of the RCA circuit varies for both the baseline FinFET and NC-FinFET. Due to the intrinsic properties of the FE material the delay of the RCA circuit is degraded by 44% which results in 5.5% energy dissipation.

5. Conclusion

In this paper, we have studied the critical selection of FE thickness to explore the device-circuit characteristics of NC-FinFET. Based on that we have observed the negative DIBL in the transfer characteristics and NDR in the output characteristics. These peculiar characteristics arise due to the coupling of FE capacitance with the drain capacitance. Negative NDR shows the hysteresis in VTCs which can be used in logic gates with higher noise margin. Also, we have compared the speed and power performance of NC-FinFET based circuit with the baseline FinFET counterparts. Our results shows that delay of the NC-FinFET based embedded inverter chain reduces by 39.56% for T_{FE} = 3 nm at C_W = 10 fF. On the other hand for 3-stage RO shows performance improvement in delay and energy for V_{DD} < 0.45 V. In case of 2 bit ripple carry adder delay decreased by 44% and improves EDP in comparison to FinFET. Overall, the delay of the NC-FinFET based embedded inverter chain, ROs and RCA significantly reduced with the increase in ferroelectric thickness. We have also found that for low frequency operation there is a significant improvement in the power ratio albeit at higher frequency the power dissipation degrades as compared to the baseline transistors.

CRediT authorship contribution statement

Rajeewa Kumar Jaisawal: Conceptualization, Writing – original draft. **P.N. Kondekar:** Supervision. **Sameer Yadav:** Methodology, Software, Data curation. **Pranshoo Upadhyay:** Validation, Writing – review & editing. **Bhaskar Awadhiya:** Visualization, Writing – review & editing. **Sunil Rathore:** Software, Investigation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

[1] J.-P. Colinge, FinFETs and Other Multi-Gate Transistors, Springer, Cham, Switzerland, 2008.
[2] J. Rabaey, Low Power Design Essentials, Springer, 2009.
[3] K. Cheng, C. Park, C. Yeung, S. Nguyen, J. Zhang, X. Miao, M. Wang, S. Mehta, J. Li, C. Surisetty, R. Muthinti, Z. Liu, H. Tang, S. Tsai, T. Yamashita, H. Bu, R. Divakaruni, Air spacer for 10 nm FinFET cmos and beyond, in: 2016 IEEE International Electron Devices Meeting, IEDM, 2016, pp. 17.1.1–17.1.4, http://dx.doi.org/10.1109/IEDM.2016.7838436.
[4] A. Wang, V. Dhawan, C.-J.R. Shi, Analog building block design in 14 nm FinFET using inversion coefficient, in: 2014 SOI-3D-Subthreshold Microelectronics Technology Unified Conference, S3S, 2014, pp. 1–3, http://dx.doi.org/10.1109/S3S.2014.7028207.
[5] S. Salahuddin, S. Datta, Use of negative capacitance to provide voltage amplification for low power nanoscale devices, Nano Lett. 8 (2008) 405–410, http://dx.doi.org/10.1021/nl071804g.
[6] A.I. Khan, C.W. Yeung, C. Hu, S. Salahuddin, Ferroelectric negative capacitance MOSFET: Capacitance tuning antiferroelectric operation, in: 2011 International Electron Devices Meeting, 2011, pp. 11.3.1–11.3.4, http://dx.doi.org/10.1109/IEDM.2011.6131532.

[7] A. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. Bakaul, R. Ramesh, S. Salahuddin, Negative capacitance in a ferroelectric capacitor, Nature Mater. 14 (2014) http://dx.doi.org/10.1038/nmat4148.

[8] A. Khan, D. Bhowmik, P. Yu, S.J. Kim, X. Pan, R. Ramesh, S. Salahuddin, Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures, Appl. Phys. Lett. 99 (2011) http://dx.doi.org/10.1063/1.3634072.

[9] B. Awadhiya, P. Kondekar, A. Meshram, Effect of ferroelectric thickness variation in undoped HfO_2-based negative-capacitance field-effect transistor, J. Electron. Mater. 48 (2019) http://dx.doi.org/10.1007/s11664-019-07483-1.

[10] S. Yadav, P. Upadhyay, B. Awadhiya, P.N. Kondekar, Design and analysis of improved phase-transition FinFET utilizing negative capacitance, IEEE Trans. Electron Devices 68 (2) (2021) 853–859, http://dx.doi.org/10.1109/TED.2020.3043222.

[11] Y. Liang, X. Li, S. George, S. Srinivasa, Z. Zhu, S.K. Gupta, S. Datta, V. Narayanan, Influence of body effect on sample-and-hold circuit design using negative capacitance fet, IEEE Trans. Electron Devices 65 (9) (2018) 3909–3914, http://dx.doi.org/10.1109/TED.2018.2852679.

[12] K. Bernstein, R.K. Cavin, W. Porod, A. Seabaugh, J. Welser, Device and architecture outlook for beyond cmos switches, Proc. IEEE 98 (12) (2010) 2169–2184, http://dx.doi.org/10.1109/JPROC.2010.2066530.

[13] G. Pahwa, T. Dutta, A. Agarwal, Y.S. Chauhan, Designing energy efficient and hysteresis free negative capacitance FinFET with negative dibl and 3.5x ion using compact modeling approach, in: 2016 46th European Solid-State Device Research Conference, ESSDERC, 2016, pp. 41–46, http://dx.doi.org/10.1109/ESSDERC.2016.7599584.

[14] G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, Y.S. Chauhan, Analysis and compact modeling of negative capacitance transistor with high on-current and negative output differential resistance—part II: Model validation, IEEE Trans. Electron Devices 63 (12) (2016) 4986–4992, http://dx.doi.org/10.1109/TED.2016.2614436.

[15] B. Awadhiya, P.N. Kondekar, A.D. Meshram, Investigating undoped HfO_2 as ferroelectric oxide in leaky and non-leaky fe-de heterostructure, Trans. Electr. and Electron. Mater. (2019) 1–6.

[16] Y. Liang, X. Li, S.K. Gupta, S. Datta, V. Narayanan, Analysis of dibl effect and negative resistance performance for NCFET based on a compact spice model, IEEE Trans. Electron Devices 65 (12) (2018) 5525–5529, http://dx.doi.org/10.1109/TED.2018.2875661.

[17] Y. Liang, Z. Zhu, X. Li, S.K. Gupta, S. Datta, V. Narayanan, Utilization of negative-capacitance FETs to boost analog circuit performances, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 27 (12) (2019) 2855–2860, http://dx.doi.org/10.1109/TVLSI.2019.2932268.

[18] Y. Li, Y. Kang, X. Gong, Evaluation of negative capacitance ferroelectric MOSFET for analog circuit applications, IEEE Trans. Electron Devices 64 (10) (2017) 4317–4321, http://dx.doi.org/10.1109/TED.2017.2734279.

[19] Y.-C. Lu, V.P.-H. Hu, Evaluation of analog circuit performance for ferroelectric soi MOSFETs considering interface trap charges and gate length variations, in: 2019 Silicon Nanoelectronics Workshop, SNW, 2019, pp. 1–2, http://dx.doi.org/10.23919/SNW.2019.8782942.

[20] Y. Liang, Z. Zhu, X. Li, S.K. Gupta, S. Datta, V. Narayanan, Mismatch of ferroelectric film on negative capacitance FETs performance, IEEE Trans. Electron Devices 67 (3) (2020) 1297–1304, http://dx.doi.org/10.1109/TED.2020.2968050.

[21] A. Aziz, S. Ghosh, S. Datta, S.K. Gupta, Physics-based circuit-compatible spice model for ferroelectric transistors, IEEE Electron Device Lett. 37 (6) (2016) 805–808, http://dx.doi.org/10.1109/LED.2016.2558149.

[22] S. George, A. Aziz, X. Li, M.S. Kim, S. Datta, J. Sampson, S. Gupta, V. Narayanan, Device circuit co design of fefet based logic for low voltage processors, in: 2016 IEEE Computer Society Annual Symposium on VLSI, ISVLSI, 2016, pp. 649–654, http://dx.doi.org/10.1109/ISVLSI.2016.116.

[23] S. George, K. Ma, A. Aziz, X. Li, A. Khan, S. Salahuddin, M.-F. Chang, S. Datta, J. Sampson, S. Gupta, V. Narayanan, Nonvolatile memory design based on ferroelectric FETs, in: 2016 53nd ACM/EDAC/IEEE Design Automation Conference, DAC, 2016, pp. 1–6, http://dx.doi.org/10.1145/2897937.2898050.

[24] N. Shukla, A. Thathachary, A. Agrawal, H. Paik, A. Aziz, D. Schlom, S. Gupta, R. Engel-Herbert, S. Datta, A steep-slope transistor based on abrupt electronic phase transition, Nature Commun. 6 (2015) 7812, http://dx.doi.org/10.1038/ncomms8812.

[25] A. Aziz, S. Ghosh, S. Datta, S.K. Gupta, Physics-based circuit-compatible spice model for ferroelectric transistors, IEEE Electron Device Lett. 37 (6) (2016) 805–808, http://dx.doi.org/10.1109/LED.2016.2558149.

[26] X. Li, J. Sampson, A. Khan, K. Ma, S. George, A. Aziz, S.K. Gupta, S. Salahuddin, M.-F. Chang, S. Datta, V. Narayanan, Enabling energy-efficient nonvolatile computing with negative capacitance FET, IEEE Trans. Electron Devices 64 (8) (2017) 3452–3458, http://dx.doi.org/10.1109/TED.2017.2716338.

[27] T.K. Song, Landau-Khalatnikov simulations for ferroelectric switching in ferroelectric random access memory application, J. Korean Phys. Soc. 46 (2005) 5–9.

[28] K. Rabe, M. Dawber, C. Lichtensteiger, C. Ahn, J.-M. Triscone, Modern Physics of Ferroelectrics: Essential Background, Vol. 105, 2007, pp. 1–30, http://dx.doi.org/10.1007/978-3-540-34591-6_1.

[29] B. Awadhiya, P. Kondekar, A. Meshram, Passive voltage amplification in non-leaky ferroelectric-dielectric hetero structure, Micro Nano Lett. 13 (2018) http://dx.doi.org/10.1049/mnl.2018.5172.

[30] Z.C. Yuan, S. Rizwan, M. Wong, K. Holland, S. Anderson, T.B. Hook, D. Kienle, S. Gadelrab, P.S. Gudem, M. Vaidyanathan, Switching-speed limitations of ferroelectric negative-capacitance FETs, IEEE Trans. Electron Devices 63 (10) (2016) 4046–4052, http://dx.doi.org/10.1109/TED.2016.2602209.

[31] Y. Li, K. Yao, G.S. Samudra, Delay and power evaluation of negative capacitance ferroelectric MOSFET based on spice model, IEEE Trans. Electron Devices 64 (5) (2017) 2403–2408, http://dx.doi.org/10.1109/TED.2017.2674020.

[32] Y. Li, K. Han, Y. Kang, E.Y.J. Kong, X. Gong, Extraction of polarization-dependent damping constant for dynamic evaluation of ferroelectric films and devices, IEEE Electron Device Lett. 39 (8) (2018) 1211–1214, http://dx.doi.org/10.1109/LED.2018.2845946.

[33] S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu, T. Ghani, M. Giles, S. Govindaraju, R. Grover, W. Han, D. Hanken, E. Haralson, M. Haran, M. Heckscher, R. Heussner, P. Jain, R. James, R. Jhaveri, I. Jin, H. Kam, E. Karl, C. Kenyon, M. Liu, Y. Luo, R. Mehandru, S. Morarka, L. Neiberg, P. Packan, A. Paliwal, C. Parker, P. Patel, R. Patel, C. Pelto, L. Pipes, P. Plekhanov, M. Prince, S. Rajamani, J. Sandford, B. Sell, S. Sivakumar, P. Smith, B. Song, K. Tone, T. Troeger, J. Wiedemer, M. Yang, K. Zhang, A 14 nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm^2 sram cell size, in: 2014 IEEE International Electron Devices Meeting, 2014, pp. 3.7.1–3.7.3, http://dx.doi.org/10.1109/IEDM.2014.7046976.

[34] Y. Chauhan, D. Lu, S. Venugopalan, S. Khandelwal, J. Duarte, N. Paydavosi, A. Niknejad, C. Hu, FinFET Modeling for IC Simulation and Design using the BSIM-CMG StandArd, 2015.

[35] K.-S. Li, P.-G. Chen, T.-Y. Lai, C.-H. Lin, C.-C. Cheng, C.-C. Chen, Y.-J. Wei, Y.-F. Hou, M.-H. Liao, M.-H. Lee, M.-C. Chen, J.-M. Sheih, W.-K. Yeh, F.-L. Yang, S. Salahuddin, C. Hu, Sub-60mv-swing negative-capacitance FinFET without hysteresis, in: 2015 IEEE International Electron Devices Meeting, IEDM, 2015, pp. 22.6.1–22.6.4, http://dx.doi.org/10.1109/IEDM.2015.7409760.

[36] G. Pahwa, T. Dutta, A. Agarwal, Y.S. Chauhan, Physical insights on negative capacitance transistors in nonhysteresis and hysteresis regimes: MFMIS versus MFIS structures, IEEE Trans. Electron Devices 65 (3) (2018) 867–873, http://dx.doi.org/10.1109/TED.2018.2794499.

[37] Arizona state university predictive technology models, 2021, URL http://ptm.asu.edu/.

[38] S. Gupta, M. Steiner, A. Aziz, V. Narayanan, S. Datta, S.K. Gupta, Device-circuit analysis of ferroelectric FETs for low-power logic, IEEE Trans. Electron Devices 64 (8) (2017) 3092–3100, http://dx.doi.org/10.1109/TED.2017.2717929.

[39] Y.-C. Lin, F. McGuire, A.D. Franklin, Realizing ferroelectric Hf0.5Zr0.5O2 with elemental capping layers, J. Vac. Sci. Technol. B 36 (1) (2018) 011204, http://dx.doi.org/10.1116/1.5002558.

[40] B. Awadhiya, P.N. Kondekar, S. Yadav, P. Upadhyay, Insight into threshold voltage and drain induced barrier lowering in negative capacitance field effect transistor, Trans. Electr. Electron. Mater. (2021) http://dx.doi.org/10.1007/s42341-020-00230-y.

[41] J. Li, B. Nagaraj, H. Liang, W. Cao, C. Lee, R. Ramesh, Ultrafast polarization switching in thin-film ferroelectrics, Appl. Phys. Lett. 84 (2004) 1174–1176, http://dx.doi.org/10.1063/1.1644917.

[42] Z.C. Yuan, S. Rizwan, M. Wong, K. Holland, S. Anderson, T.B. Hook, D. Kienle, S. Gadelrab, P.S. Gudem, M. Vaidyanathan, Switching-speed limitations of ferroelectric negative-capacitance FETs, IEEE Trans. Electron Devices 63 (10) (2016) 4046–4052, http://dx.doi.org/10.1109/TED.2016.2602209.