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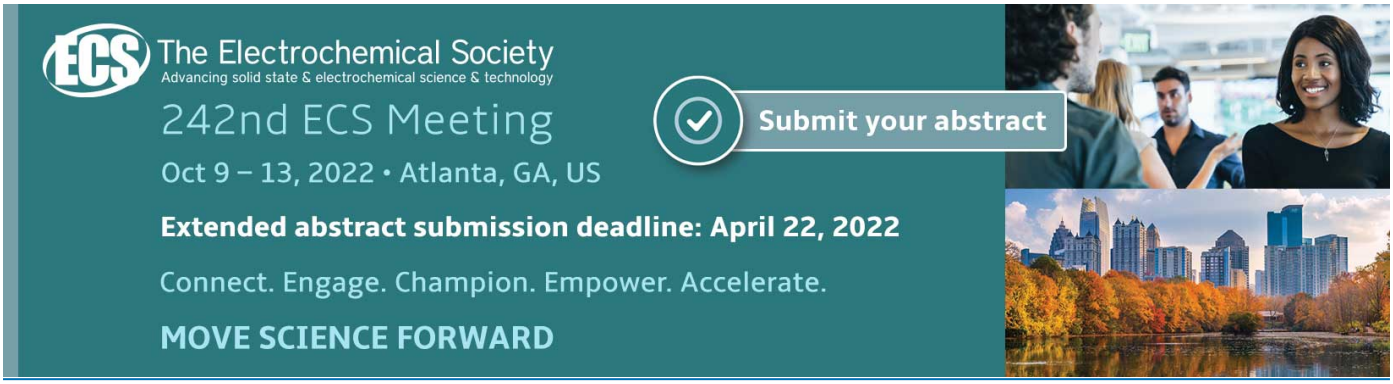

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Assessing the analog/RF and linearity performances of FinFET using high threshold voltage techniques

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Abstract

One of the severe issues of the downscaling of semiconductor devices is the threshold voltage reduction which significantly increases the leakage current. Thus, high threshold voltage (HVT) techniques are required to bring down the leakage hike for improved performances. In this paper, for the first time, we investigate the analog/radio frequency (RF) and linearity performances of silicon (Si) FinFET by employing HVT techniques. Using well-calibrated technology computer aided design models, to mitigate the leakage current, we analyzed the following approach to get HVT: (a) increasing channel doping ($N_{ch'}$); (b) making drain-side underlap (L_{dsu}); (c) increasing gate length ($L_{g'}$). Two flavors of fin field effect transistors (FinFETs) viz bulk and silicon-on-insulator (SOI) are suitably compared over their baseline counterpart, i.e. without HVTs. A thorough investigation of analog/RF metrics such as transconductance, output resistance, gate capacitance, cut-off frequency, gain-bandwidth, and transconductance-frequency product proves the eminence of bulk-FinFET over its peer SOI-FinFET. In contrast, SOI-FinFET shows merits in intrinsic gain and linearity such as g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3, IMD_3, and 1 dB compression point. Thus, HVT techniques are worth analyzing for a FinFET architecture employed in analog/RF applications.

Keywords: FinFET, high threshold voltage, leakage current, analog/RF, linearity, silicon-on-insulator

(Some figures may appear in color only in the online journal)

1. Introduction

Fin field effect transistor (FinFET)-based complimentry metal oxide semiconductor (CMOS) logic devices are attaining popularity due to their high performance, low power, improved gate electrostatic, superior scalability, and low subthreshold slope (SS) when compared to the conventional FETs [1–4]. FinFETs fabricated on silicon-on-insulator (SOI) substrates can suppress sub-fin leakage current while exhibiting excellent subthreshold swing [5]. Using punch-through stopper (PTS) doping beneath the channel fin region, the device characteristics and performance of bulk FinFET can be matched with those of SOI-FinFET [6]. Modern communication systems operating in the gigahertz frequency range require the low intermodulation linear operation of FinFET based CMOS devices to detect the weak signal [7, 8]. A substantial experiment and mitigation of nonlinearity present in the output characteristics of the FinFET based devices are necessitated

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for the high-frequency application, which is both costly and time-demanding. Therefore, the linearity is analyzed in terms of quite efficient and less arduous metrics like g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3, IMD_3, and 1 dB compression point, which is ensured that the higher-order harmonics and intermodulation distortion are minimized at the output of the radio frequency (RF) systems. According to International Technology Roadmap of Semiconductor (ITRS), evaluating the device's analog/RF and linearity figure of merits (FoMs) for application perspective is vital [9]. FinFET devices have higher intrinsic gain for low-frequency applications compared to bulk metal oxide semiconductor field effect transistors (MOSFETs); however, exhibit inferior frequency behavior for high-frequency applications due to higher series resistance and lower carrier mobility along the channel sidewalls [10, 11]. The RF performance of FinFET is a strong function of gate length (L_g) and fin width (F_w), and the unity gain cut-off frequency (f_T) of FinFET improves as F_w increases [12].

Therefore, it is necessary to investigate the maximum f_T of the leading-edge devices like FinFETs. Recently, the RF performance parameters in terms of the maximum operating frequency (f_{max}) and f_T of the FinFET have been investigated [13–15]. However, the leakage current, analog/RF, and linearity performance parameters of high threshold voltage (HVT) and low threshold voltage (LVT), i.e. baseline bulk and SOI FinFETs, have not been explored yet.

In this paper, using well-calibrated technology computer aided design (TCAD) models for 14 nm technology node [16], the impact of HVT techniques such as increasing channel doping concentration ($N_{ch'}$), drain-side underlap (L_{dsu}), and increasing channel length ($L_{g'}$) on leakage current, analog/RF, and linearity performance of bulk-FinFET and SOI-FinFET have been studied.

Our key contribution: In this paper, the following key evolved ideas and objectives are setups for HVT-FinFET device analysis:

- Investigation of different HVT techniques in bulk-FinFET and SOI-FinFET, separately.
- The impact of HVT techniques in leakage current improvement of bulk-FinFET and SOI-FinFET is studied to enable enhanced standby power performance.
- Analog/RF and linearity analysis of HVT-FinFETs.
- A proper comparison of all the HVT techniques and provided optimized device guidelines.

The rest of the paper is organized as follows: in section 2, the TCAD simulation methodology, device calibration, and baseline (LVT) bulk and SOI FinFET device characteristics are discussed. Section 3 investigates the HVT techniques and their impact on analog/RF and linearity FoMs of bulk and SOI FinFETs, respectively. Finally, a summary is drawn in section 4.

2. Device structure and simulation methodology

Three dimensional (3D) schematic of the bulk-FinFET and SOI-FinFET are shown in figures 1(a) and (b), and the cross-section view is shown in figures 1(c) and (d), respectively. The device consists of SiO_2 as the interfacial oxide layer and HfO_2 as the high-k gate dielectric material. Metal as the gate electrode and the spacer (Si_3N_4) to suppress the gate-drain/source capacitances [17, 18]. To obtain the reliable TCAD simulation results, the baseline bulk-FinFET [19] and SOI-FinFET [20] are carefully calibrated with the reported experimental data. Table 1 articulates the device parameters used for device calibration. For a fair comparison, the uniform doping 10^{20} cm^{-3} of phosphorous in source/drain (S/D) pads and 10^{16} cm^{-3} of boron in the channel region is used in bulk and SOI FinFET [21]. The S/D is highly doped to alleviate leakage current and mitigate the effect of the drain induced barrier lowering (DIBL) and random doping fluctuation [22]. TCAD simulation framework includes various device physics models tuned in the prescribed range to match the experimental data well. Shchokley–Read–Hall (SRH) model for incorporating carrier generation and recombination. The quantum-potential and drift-diffusion transport models render the device's electrical performance, such as currents and terminal charges. The carrier mobility behavior has been captured by incorporating the Caughey–Thomas model for high field saturation, Lombardi model to alleviate mobility degradation due to high-k dielectric [23], ballistic mobility model to study short channel effects, and doping dependent (UniBo) model to account for lattice scattering and electron–hole scattering [24]. Finally, the work function of the metal gate electrode (TiN) and the S/D contact resistances are adjusted to calibrate the transfer characteristics (I_{DS}–V_{GS}), as shown in figure 2. At low drain bias and high drain bias, the bulk-FinFET has a linear drive current $I_{DS,lin}$ of 0.24 mA μm^{-1}, and a saturation current $I_{DS,sat}$ of 1.1 mA μm^{-1}, respectively. Similarly, the SOI-FinFET exhibits linear drive current $I_{DS,lin}$ of 0.11 mA μm^{-1}, and

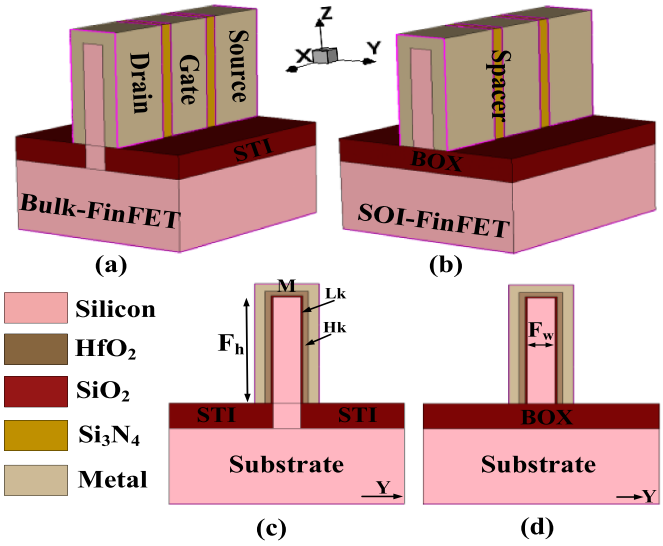

Figure 1. Three-dimensional structure illustration of (a) Si bulk-FinFET, (b) SOI-FinFET, and cross-sectional view of (c) Si bulk-FinFET, (d) SOI-FinFET. Both flavors of FinFETs have equivalent dimensions chosen for a fair comparison, as mentioned in table 1.

Table 1. Parameters table.

Symbol	Parameters	Bulk FinFET	SOI FinFET
L_g	Channel length	20 nm	20 nm
F_h	Fin height	42 nm	42 nm
F_w	Fin width	8 nm	8 nm
$L_{S/D}$	Source/drain length	30 nm	30 nm
L_{SP}	Spacer length	7.5 nm	7.5 nm
T_{STI}	Shallow trench isolation thickness	10 nm	—
T_{BOX}	Buried oxide thickness	—	10 nm
T_{EOT}	Equivalent oxide thickness	0.9 nm	0.9 nm
ε_{ox}	Gate dielectric (HfO_2)	$22\varepsilon_o$	$22\varepsilon_o$
ε_{sp}	Spacer dielectric (Si_3N_4)	$7.5\varepsilon_o$	$7.5\varepsilon_o$
N_{ch}	Channel doping	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
N_{SD}	Source/drain doping	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
N_{PTS}	Punch through stopper doping	5×10^{17} cm^{-3}	—
N_{sub}	Substrate doping	5×10^{17} cm^{-3}	5×10^{17} cm^{-3}

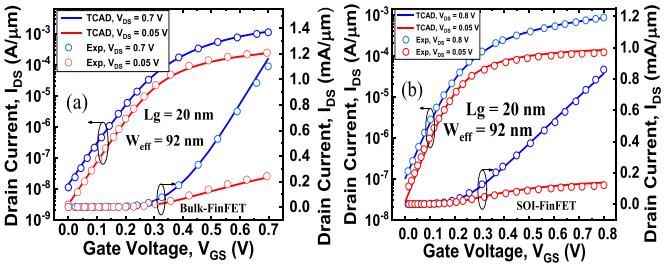

Figure 2. Transfer characteristics (I_{DS}–V_{GS}) of (a) Si bulk-FinFET with the experimental data [19] and (b) SOI-FinFET with the experimental data [20]. We have separately calibrated the baseline bulk-FinFET and SOI-FinFET with appropriate tuning parameters and taken similar doping profiles for a fair comparison.

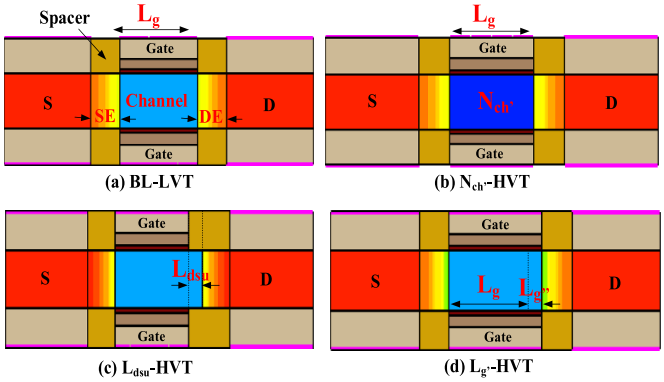

Figure 3. Contour plots of (a) baseline LVT-FinFET ($L_g = 20$ nm), (b) HVT-FinFET with increased channel doping ($N_{ch'} = 2 \times 10^{18}$ cm^{-3}), (c) HVT-FinFET with drain-side underlap ($L_{dsu} = 4$ nm), and (d) HVT-FinFET with increased gate length ($L_{g'} = L_g + L_{g''} = 24$ nm). SE and DE represent the source and drain extension region, respectively.

saturation current $I_{DS,sat}$ of 0.868 mA μm^{-1}, respectively. Note that the drain current of bulk-FinFET and SOI-FinFET has been normalized by effective channel width, given as $W_{eff} = 2F_h + F_W$.

3. Results and discussion

This paper investigated the impact of incorporating the HVT techniques on analog/RF performance of bulk- and SOI FinFETs. The inversion electron density across the channel region reveals that the peak electron charge density of the bulk- and SOI FinFET are 1×10^{19} cm^{-3} and 8×10^{19} cm^{-3}, respectively. This peak value of the charge centroid is situated at the middle of the fin because strong 2D quantum confinement along the fin width causes volume inversion [25]. Figure 3 shows the contour plots of LVT baseline FinFET (figure 3(a)) and HVT FinFETs with increased channel doping concentration ($N_{ch'}$) (figure 3(b)), drain-side underlap ($L_{dsu} = 4$ nm) (figure 3(c)), and increased gate length ($L_{g'} = 24$ nm) (figure 3(d)).

3.1. Leakage current analysis

Devices with multi-threshold voltages (V_{th}) are frequently required for power performance improvement [26, 27]. HVT-FinFETs devices have the advantage of optimized power performance due to improved leakage current compared to the LVT, i.e. baseline FinFETs. HVT-FinFET can be designed with either: (a) increased channel doping concentration ($N_{ch'}$) (figure 3(b)), which in turn increases the V_{th}. (b) Creating an underlap at the drain side, which increases the depletion width and, in turn, reduces the inversion carrier density and increases the output resistance. Therefore, V_{th} could be improved. The concept of asymmetric gate-source/drain underlap (L_{dsu}) (figure 3(c)) has been implemented in a static random access memory to achieve adjustable V_{th}, improved $I_{OFF,}$ and stability [28, 29]. (c) Similarly, a fraction increase in channel length (i.e. $L_{g'}$) increases the $V_{th,}$ and it is a

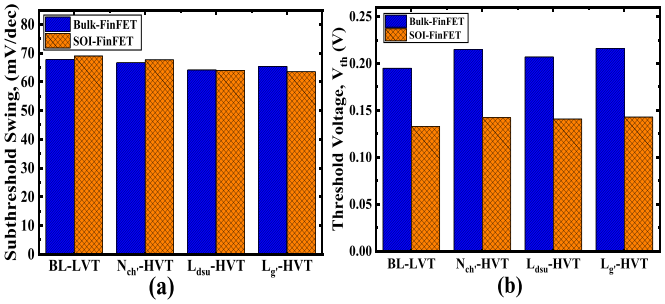

Figure 4. Impact of incorporating different HVT techniques in bulk-FinFET and SOI-FinFET on (a) subthreshold swing (SS); and (b) threshold voltage (V_{th}).

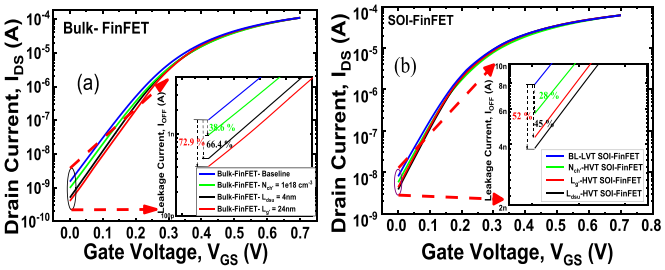

Figure 5. Impact of L_{dsu}, $L_{g'}$, and $N_{ch'}$ HVT techniques on the leakage current of (a) bulk-FinFET and (b) SOI-FinFET keeping the same ON current, and fixed V_{DS} of 0.7 V. Results reveal that L_{dsu}-HVT is the most effective way to suppress the I_{OFF} in both bulk-FinFET and SOI-FinFET.

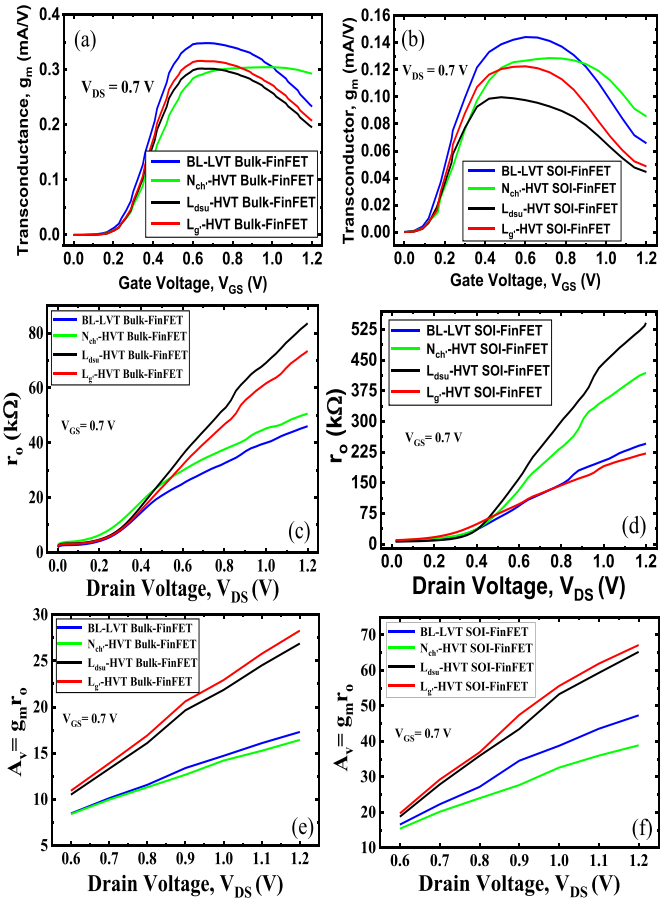

Figure 6. Illustration of the impact of incorporating various HVT techniques on transconductance (g_m) (a), (b), output resistance (r_0) (c), (d) and on intrinsic gain (e), (f) of the bulk-FinFET (a), (c), (e), and SOI-FinFET (b), (d), (f), respectively.

widely adopted approach in microprocessor designs [30]. The drain current of HVT techniques improves in the subthreshold region, which demarcates high V_{GS} is necessitated to turn ON the HVT-FinFET. Hence, the threshold voltage increases for HVT-FinFET compared to LVT-FinFET (figure 4(b)). Here, V_{th} is calculated by using the constant current method [22]. Figure 4 shows the effect of different HVT techniques on subthreshold swing and threshold voltage of bulk and SOI FinFET. The subthreshold swing of L_{dsu}, $L_{g'}$, and $N_{ch'}$ HVT-FinFETs improves by 5.2%, 3.53%, and 1.56%, respectively, compared to LVT bulk-FinFET. Similarly, by using L_{dsu}, $L_{g'}$, and $N_{ch'}$ techniques in HVT SOI-FinFET subthreshold swing enhanced by 7.2%, 7.9%, and 1.92%, respectively, compared to LVT SOI-FinFET. Thus, L_{dsu}-HVT improves the subthreshold swing better compared with other HVT techniques for both bulk-FinFET and SOI-FinFET. Figures 5(a) and (b) summarizes the comprehensive I_{DS}–V_{GS} characteristics of bulk-FinFET and SOI-FinFET by incorporating the different HVT techniques. The aforementioned parameters have a significant impact on leakage current improvement. With the adoption of $L_{g'}$-HVT, $N_{ch'}$-HVT, and L_{dsu}-HVT the leakage current of LVT bulk-FinFET improves by 38.6%, 66.4%, and 72.9%, respectively (figure 5(a)). Similarly, for LVT SOI-FinFET, it improves by 45%, 28%, and 52%, respectively (figure 5(b)).

3.2. Analog/RF analysis

In this sub-section, we thoroughly investigated the analog/RF performance parameters of the proposed HVT-FinFET and compared them with the baseline LVT-FinFET. In this manuscript, we have analyzed various parameters such as transconductance (g_m), output resistance (r_0), intrinsic gain ($g_m r_0$), unity gain cut-off frequency (f_T), total gate capacitance (C_{gg}), transconductance frequency product (TFP), and gain-bandwidth product (GBP) [31]. The transconductance ($g_m = \partial I_{DS}/\partial V_{GS}$) is indeed a vital parameter worth needing for analog circuits. On similar grounds, the intrinsic gain of any circuit is a function of the transconductance and the output resistance ($r_0 = \partial I_{DS}/\partial V_{DS}$), i.e. $A_v = g_m r_0$, which would be as high as possible for better analog performance. Figure 6 shows the g_m, r_0, and A_v variation with varying gate and drain bias for the bulk- and SOI FinFET. The peak value of g_m varies with the value of V_{GS}. LVT, i.e. baseline bulk-FinFET and SOI-FinFET shows higher g_m in weak to moderate inversion regimes compared to the HVT bulk-FinFET and SOI-FinFET. Among all the HVT techniques, the $N_{ch'}$-HVT bulk-FinFET and SOI-FinFET offer higher g_m at the strong inversion regime. However, the intrinsic gain of the

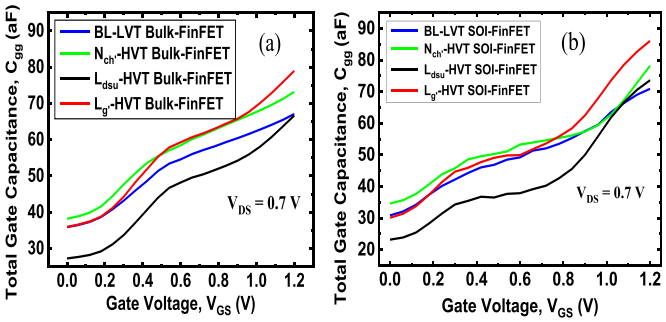

Figure 7. The total gate capacitance (C_{gg}) of the (a) bulk-FinFET and (b) SOI-FinFET with varying gate voltage.

HVT techniques has been improved over the LVT counterpart predominately due to the output resistance (r_0). This stands for the improved saturation region of I_D–V_{DS} characteristics, another advantage for analog circuits. Figure 7 shows the total gate capacitance (C_{gg}) of bulk-FinFET and SOI-FinFET. Compared to their counterpart baseline devices, the HVT techniques significantly impacted C_{gg} of both bulk-FinFET and SOI-FinFET. For L_{dsu}-HVT, bulk-FinFET and SOI-FinFET C_{gg} decreases as V_{th} increases in the subthreshold inversion region whereas, for $L_{g'}$-HVT, bulk-FinFET and SOI-FinFET C_{gg} increases in the strong inversion region due to the charge accumulation.

The frequency where the short circuit current gain equals one is known as the unity gain cut-off frequency (f_T) and is given as [32]:

$$f_T = \frac{g_m}{2\pi C_{gg}} = \frac{g_m}{2\pi \times (C_{gs} + C_{gd})} \tag{1}$$

where C_{gg} is the total gate capacitance, C_{gs} is gate-to-source capacitance, and C_{gd} is the gate-to-drain capacitance extracted at 1 MHz frequency [33] by applying the small alternating current (AC, i.e. sinusoidal) signal in the mixed-mode simulation. Also, it is assumed that body is connected to the source. From equation (1), it is clear that f_T is a strong function of g_m and C_{gg}. Figures 8(a) and (b) depicts the unity gain cut-off frequency of bulk-FinFET and SOI-FinFET for LVT and HVT techniques, respectively. Compared with LVT bulk-FinFET, the peak values of f_T diminished by 22%, 7%, and 16%, for $N_{ch'}$-HVT, L_{dsu}-HVT, and $L_{g'}$-HVT bulk-FinFET, respectively (figure 8(a)). Similarly, for LVT SOI-FinFET, the peak value of f_T decreased by 17%, 5%, and 19% for $N_{ch'}$-HVT, L_{dsu}-HVT, and $L_{g'}$-HVT SOI-FinFET, respectively (figure 8(b)). The decrease in the value of g_m for weak and moderate inversion regions is the root cause of the decreases in f_T. As a result, the RF performance of HVT bulk-FinFET and SOI-FinFET degrades compared with LVT bulk-FinFET and SOI-FinFET. The GBP can be given as [34]:

$$\text{GBP} = \frac{g_m}{2\pi \times 10 \times C_{gd}}. \tag{2}$$

Figures 8(c) and (d) shows the GBP and TFP of HVT bulk-FinFET and SOI-FinFET compared with LVT-FinFETs, respectively. The GBP of HVT bulk-FinFET is decreased

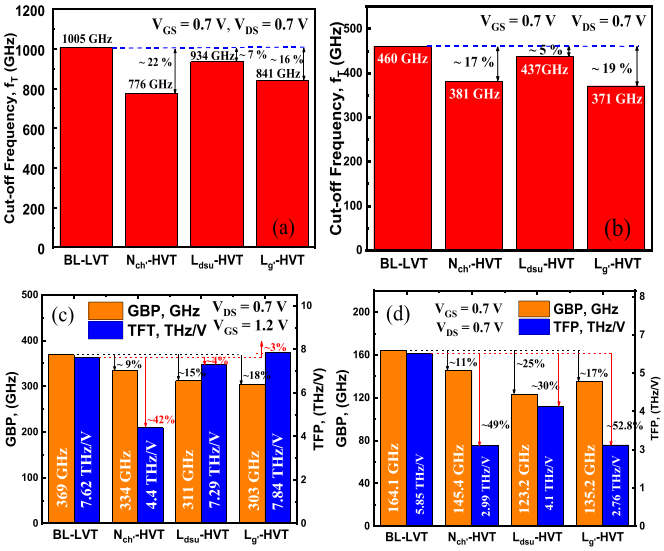

Figure 8. Illustration of the impact of incorporating various HVT techniques on unity gain cut-off frequency (f_T) (a), (b), GBP and TFP (c), (d) of bulk-FinFET (a), (c), and SOI-FinFET (b), (d), respectively.

by 9% for $N_{ch'}$-HVT bulk-FinFET, 15% for L_{dsu}-HVT bulk-FinFET, and 18% for $L_{g'}$-HVT bulk-FinFET as compared with LVT bulk-FinFET. Similarly, for HVT SOI-FinFET, it decreases by 11% ($N_{ch'}$-HVT), 25% (L_{dsu}-HVT), and 17% ($L_{g'}$-HVT) with respect to LVT SOI-FinFET. The GBP of LVT bulk-FinFET and LVT SOI-FinFET is 369 and 164 GHz, respectively, making them quite appropriate for gigahertz applications. The TFP predicts the comprehensive analog/RF performance of FinFET as [34]:

$$\text{TFP} = \left(\frac{g_m}{I_{DS}}\right) \times f_T. \tag{3}$$

TFP of HVT bulk-FinFET decreases for $N_{ch'}$-HVT and L_{dsu}-HVT by 42%, 4%, respectively, but for $L_{g'}$-HVT, it increases by 3%, as well compared to LVT bulk-FinFET (figure 8(c)). However, for $N_{ch'}$-HVT, L_{dsu}-HVT, and $L_{g'}$-HVT SOI-FinFET, TFP decreases by 49%, 30%, and 52.8%, respectively, as compared to LVT SOI-FinFET (figure 8(d)). TFP deteriorate for HVT bulk-FinFET and SOI-FinFET because the peak value of g_m and f_T decreases compared to LVT bulk-FinFET and SOI-FinFET. Thus, the overall analog/RF performance of HVT bulk-FinFET and SOI-FinFET degrades as compared to LVT bulk-FinFET and SOI-FinFET for RF applications with a sounding improvement in the leakage current.

3.3. Linearity performance and distortion analysis

This sub-section investigates the linearity and harmonic distortion of bulk and SOI FinFETs with and without HVT techniques. In general, the minimum harmonic distortion of devices would provide power saving in RF communication. To study the distortion and linearity of the LVT and HVT-FinFETs, numerous metrics have been explored such as

g_{m2} (second-order harmonics transconductance), g_{m3} (third-order harmonics transconductance), VIP_2 (interpolated input voltage where first-order harmonic voltage is equal to second-order harmonics voltage), VIP_3 (interpolated input voltage where first-order harmonic voltage is equal to third-order harmonics voltage), IIP_3 (third-order input power intercept point), IMD_3 (third-order intermodulation distortion), and 1 dB compression point, etc [35].

The linearity and distortion FoMs of the preceding terms can be calculated as:

$$VIP_2 = 4 \times \left(\frac{g_{m1}}{g_{m2}}\right) \tag{4}$$

$$VIP_3 = \sqrt{24 \times \left(\frac{g_{m1}}{g_{m3}}\right)} \tag{5}$$

$$IIP_3 = \frac{2}{3} \times \left(\frac{g_{m1}}{g_{m3} \times R_S}\right) \tag{6}$$

$$IMD_3 = \left[\frac{9}{2} \times \left((VIP_3)^3 \times g_{m3}\right)\right]^2 \times R_S \tag{7}$$

$$1-\text{dB compression point} = 0.22 \times \sqrt{\left(\frac{g_{m1}}{g_{m3}}\right)} \tag{8}$$

where, $g_{mn} = \partial^n I_{DS}/\partial V_{GS}{}^n$, $n = 1, 2, 3$ are the first, second, and third-order derivatives of drain current with respect to drain voltage and $R_S = 50\ \Omega$ is opted [35]. Figure 9 depicts the variation of g_{m2} and g_{m3} with respect to the gate voltage for bulk and SOI FinFET. The peak value of g_{m2} and g_{m3} should be lower and the zero crossover point of g_{m3} should occur at lower V_{GS} for better linearity performance. Here, the value of V_{GS} where g_{m3} tries the first zero occurs is defined as the zero crossover point. The values of g_{m2} and g_{m3} are lower for $N_{ch'}$-HVT bulk-FinFET and SOI-FinFET (figure 9), indicating improved linearity performance. To design a device for better linearity performance with less distortion, IIP_3, VIP_2, and VIP_3 values should be maximum, and IMD_3 should be minimum [35]. Figures (10)–(12) shows the variation of different linearity FoMs with respect to V_{GS} at constant $V_{DS} = 0.7$ V for bulk-FinFET and SOI-FinFET. Figures 10(a) and (c) shows that VIP_2 and VIP_3 attain the higher peak values, which correspond to moderate and strong inversion regions for $N_{ch'}$-HVT bulk-FinFET and L_{dsu}-HVT bulk-FinFET, respectively. Figures 10(b) and (d) shows that VIP_2 and VIP_3 attain higher peak values for $N_{ch'}$-HVT SOI-FinFET. Thus, the linearity performance of HVT bulk-FinFET and HVT SOI-FinFET is better compared to that of LVT bulk-FinFET and LVT SOI-FinFET.

IIP_3 and IMD_3 describe the extrapolated input power and intermodulation power when the first-order harmonic power equals the third-order power harmonic. Figures 11(a) and (b) exhibit that IIP_3 of bulk-FinFET and SOI-FinFET attains a higher peak value for L_{dsu}-HVT bulk-FinFET and $N_{ch'}$-HVT SOI-FinFET, respectively. In figures 11(c) and (d), $L_{g'}$-HVT FinFET has the lower value for bulk-FinFET and SOI-FinFET,

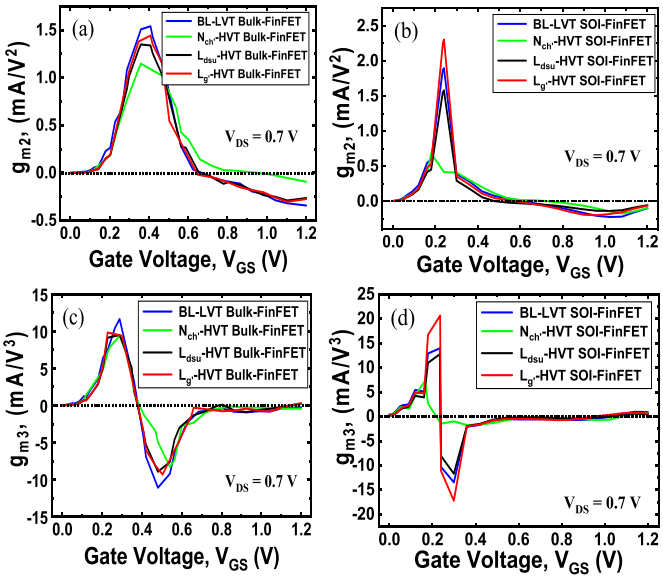

Figure 9. Illustration of the impact of different HVT techniques on second-order transconductance harmonics (g_{m2}) (a), (b) and third-order transconductance harmonics (g_{m3}) (c), (d) of bulk-FinFET (a), (c) and SOI-FinFET (b), (d).

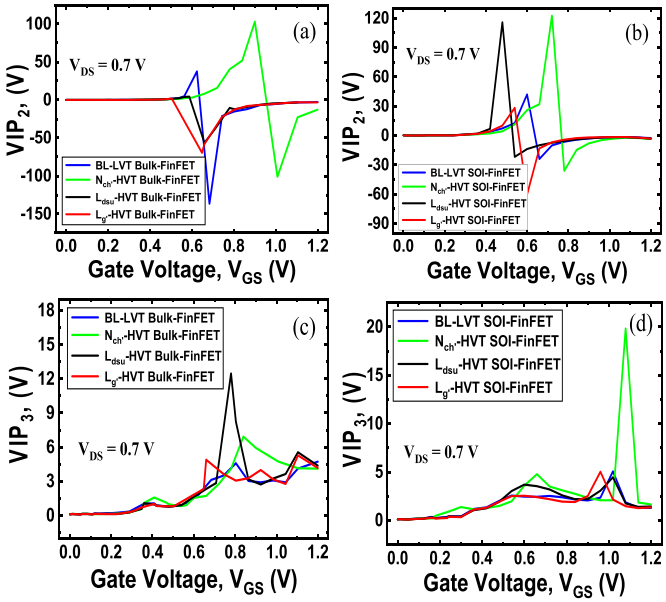

Figure 10. Illustration of the impact of different HVT techniques on VIP_2 (a), (b) and VIP_3 (c), (d) of bulk-FinFET (a), (c) and SOI-FinFET (b), (d), respectively.

indicating that $L_{g'}$-HVT technique will produce minimal distortion.

The 1 dB compression point determines the upper limit of the linearity and signifies the power level where the gain is reduced by 1 dB from its small-signal input value. Figure 12 depicts the variation of the 1 dB compression point for bulk-FinFET and SOI-FinFET. It is observed that the 1 dB compression point for $N_{ch'}$-HVT bulk-FinFET and $N_{ch'}$-HVT SOI-FinFET is high for the moderate to

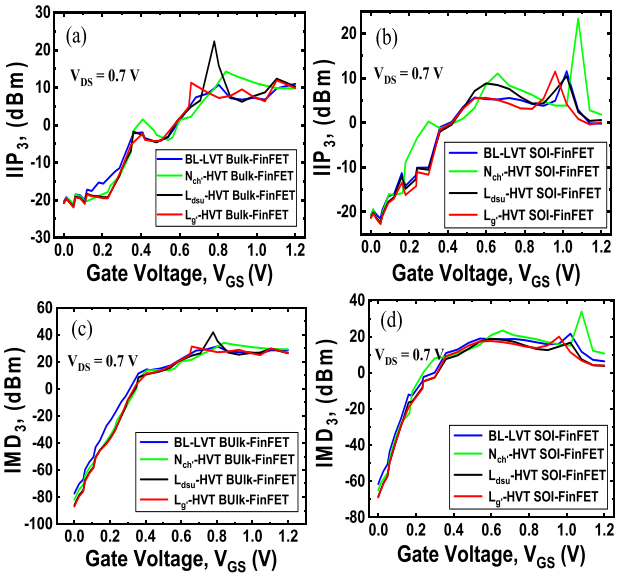

Figure 11. Illustration of the impact of different HVT techniques on IIP_3 (a), (b) and IMD_3 (c), (d) of bulk-FinFET (a), (c), and SOI-FinFET (b), (d), respectively.

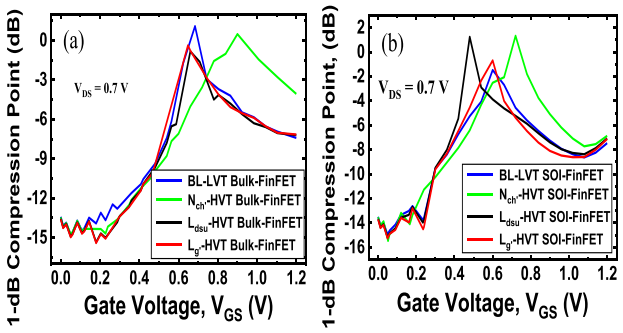

Figure 12. Illustration of the impact of HVT techniques on 1 dB compression point of (a) bulk-FinFET and (b) SOI-FinFET.

Table 2. Comprehensive analog/RF and linearity performance parameters of bulk-FinFET.

Parameter	L_g-LVT	$N_{ch'}$-HVT	L_{dsu}-HVT	$L_{g'}$-HVT
I_{OFF} (nA)	1.5	0.501	0.41	0.98
SS (mV dec^{-1})	67.73	66.67	64.16	65.34
V_{th} (V)	0.195	0.215	0.207	0.216
I_{ON}/I_{OFF} (10^5)	0.73	2.17	2.19	1.12
$A_v = g_m r_0$	17.30	16.43	26.87	28.28
C_{gg} (aF)	67.07	73.19	66.65	78.98
C_{gd} (aF)	25.66	23.69	33.6	33.86
f_T (GHz)	1005	776	934	841
GBP (GHz)	369	334	311	303
TFP (THz)	7.62	4.4	7.29	7.84
Linearity performance FoMs				
g_m (mA V^{-1})	0.348	0.305	0.302	0.316
g_{m2} (mA V^{-2})	1.54	1.15	1.35	1.44
g_{m3} (mA V^{-3})	11.65	9.37	9.5	9.8
VIP_2 (V)	37.52	103.05	4.41	1.93
VIP_3 (V)	4.59	6.93	12.46	5.29
IIP_3 (dBm)	10.69	14.26	22.29	11.92
IMD_3 (dBm)	−77.39	−82.02	−86.12	−87.08
1 dB (dB)	1.08	0.488	−0.82	−0.78

Table 3. Comprehensive analog/RF and linearity performance parameters of SOI-FinFET.

Parameter	L_g-LVT	$N_{ch'}$-HVT	L_{dsu}-HVT	$L_{g'}$-HVT
I_{OFF} (nA)	7.91	5.69	3.82	4.33
SS (mV dec^{-1})	69	67.67	64.04	63.54
V_{th} (V)	0.133	0.142	0.141	0.143
I_{ON}/I_{OFF} (10^4)	0.77	1.06	1.58	1.41
$A_v = g_m r_0$	47.33	38.87	65.23	67.15
C_{gg} (aF)	70.92	78.22	73.64	86.06
C_{gd} (aF)	41.27	45.64	51.43	52.23
f_T (GHz)	460	381	437	371
GBP (GHz)	164.1	145.4	123.2	135.2
TFP (THz)	5.85	2.99	4.1	2.76
Linearity performance FoMs				
g_m (mA V^{-1})	0.144	0.129	0.123	0.1
g_{m2} (mA V^{-2})	1.9	0.13	1.58	2.3
g_{m3} (mA V^{-3})	12.9	7.36	11	20.68
VIP_2 (V)	41.96	122.43	115.7	28.45
VIP_3 (V)	5.07	19.84	4.46	2.55
IIP_3 (dBm)	11.55	23.38	10.44	11.47
IMD_3 (dBm)	−61.55	−65.01	−68.54	−68.89
1 dB (dB)	−1.47	1.33	1.25	0.68

strong inversion regime. Thus, $N_{ch'}$-HVT technique provides improved linearity performance. For a fair comparison, the acquired results obtained by applying HVT techniques with their LVT counterparts are tabulated in table 2 for bulk-FinFET and in table 3 for SOI-FinFET, respectively. Thus, through detailed investigations, this manuscript provides a proper design guideline to suppress the leakage current and improve the analog/RF and linearity performances using HVT techniques.

4. Conclusion

Using well-calibrated TCAD models, this work investigates the impact of HVT techniques on leakage current, analog/RF, and linearity performances of bulk and SOI FinFET. Three HVT techniques, such as varying channel doping, creating drain underlap, and increasing the effective gate length, have been examined to mitigate the leakage current of the FinFET devices. Comprehensive analysis reveals that the bulk-FinFET has superior analog/RF performances than the SOI-FinFET. However, SOI-FinFET shows better linearity FoMs in terms of g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3, and IMD_3 as compared to HVT bulk-FinFET. Thus, the proposed study provides a detailed design guideline for the suitable FinFET architecture to get an insight into analog/RF applications and linearity performances.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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