

Reliability of TCAD study for HfO₂-doped Negative capacitance FinFET with different Material-Specific dopants

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ARTICLE INFO

Keywords:

Negative Capacitance
Landau Parameters
Ferroelectric Material
FinFET
HfO₂- dopants

ABSTRACT

Attaining the ferroelectric (FE) polarization in a thin HfO₂ layer using a specific dopant is a widely adopted way to realize Negative Capacitance (NC) FET. In a general TCAD simulation study of NC-based devices, the NC property of the FE layer is strongly dependent on the values of Landau parameters ($\alpha, \beta, \gamma, \rho, g$), which are unique for specific dopants and FE thickness. In this paper, for the first time, we investigated the reliability of TCAD simulations with which NC FinFET is simulated for a specific dopants-based FE-HfO₂ layer. The possible dopants used to realize a thin-HfO₂ layer as a FE layer are Al, Gd, La, Si, Sr, Y, and Zr. Each dopant has different ($\alpha, \beta, \gamma, \rho, g$) and thus offers a different NC regime of operation, i.e., S-curve. α and β are the dominant parameters if we consider the uniform polarization under quasi-static analysis. Further, the change in ambient temperature alters the value of α , resulting in changes in the NC-state. Hence, for the reliable TCAD-based NC study, the precise selection of Landau parameters and dopants is needed for optimized performances.

1. Introduction

In sub-22 nm node, FinFETs-based CMOS devices have gained popularity due to enhanced gate electrostatic controllability, subsided short channel effects (SCEs), and better power performance compared to conventional planar MOSFET [1–3]. However, the physical mechanism of the carrier transport imposes a limit of 60 mV/decade on the sub-threshold slope (SS) at room temperature (300 K). Thus, to realize a steeper-slope device, the idea of NC was reported and implemented using FE-layer in the gate stack. Employing a ferroelectric (FE) layer along with the dielectric (DE) layer in the gate stack provides a stabilized NC operation, which induces internal voltage amplification, resulting in improved gate electrostatics. Hence, the device will exhibit steep slope characteristics [4–7]. In downscaled devices, the realization of the conventional perovskite materials is not feasible due to their larger thicknesses, incompatibility with the conventional fabrication process, and environmental issues. Thus, the doped-HfO₂ layer is implemented to realize a thin film FE layer for compatible process integration [8,9]. The doped-HfO₂ layer offers significantly high remanent polarization up to 45 $\mu\text{C}/\text{cm}^2$ and a large coercive electric field ($\sim 1\text{--}2$ MV/cm). To the best of our knowledge, in the available literature, to create a thin film doped-HfO₂ FE layer, seven different dopants are used: D₁: Aluminum (Al) [P_r

= 5, E_C = 1.3]; D₂: Gadolinium (Gd) [P_r = 20, E_C = 1.75]; D₃: Lanthanum (La) [P_r = 45, E_C = 1.2]; D₄: Silicon (Si) [P_r = 10, E_C = 1.0]; D₅: Strontium (Sr) [P_r = 23, E_C = 2.0]; D₆: Yttrium (Y) [P_r = 24, E_C = 1.2]; and D₇: Zirconium (Zr) [P_r = 18, E_C = 1.0]. The P_r and E_C are in $\mu\text{C}/\text{cm}^2$ and MV/cm, respectively. In general, Hf_{0.5}Zr_{0.5}O₂-based ferroelectric material exhibits better compatibility with the CMOS devices due to equal atomic radius of Hf and Zr atoms and lower thermal transition integration (400–600 °C) [9]. Thus, in the TCAD simulation of NC devices, the dopant-dependent Landau parameters are taken. However, a thorough investigation of the reliability and optimization of these parameters, i.e., the choice and significance of the dopants for the HfO₂ layer to convert into the FE layer, is not yet explored.

The key contribution of the work explores: (i) the impact of different Landau parameters ($\alpha, \beta, \gamma, \rho, g$) for uniform FE layer under quasi-static operation; (ii) the impact of temperature on α and its significance on the NC-regime, i.e., S-curve; (iii) the impact of temperature on the trans-conductance and drivability over different dopant-dependent FE layer; (iv) the capacitance matching and its variation with varying temperature. Thus, a proper investigation is needed to select the dopant of the HfO₂-layer for optimal NC operation.

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<https://doi.org/10.1016/j.sse.2022.108531>

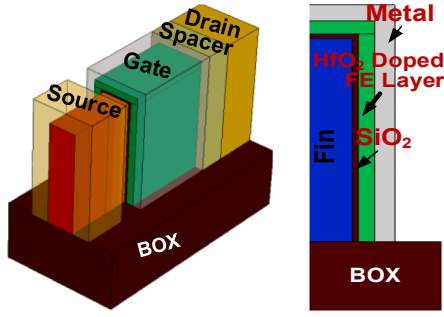


Fig. 1. Schematic of an NC-FinFET realized by placing a doped-HfO₂ ferroelectric (FE) layer at the gate stack.

2. TCAD setup for NC-FinFET

A 14 nm industry-standard FinFET is employed to realize the baseline NC-FinFET using *Sentaurus* TCAD [10] by placing the Zr-doped HfO₂ layer in the gate stack (Fig. 1). The TCAD setup includes a conventional drift–diffusion model for carrier transport. The mobility, saturation velocity, SRH recombination, high field saturation, quantum correction models, etc., have been included and adequately tuned to get a good match in I_{DS} - V_{GS} curves (Fig. 2a) between the simulated TCAD results

and experimental data [11]. The various device parameters used in the simulation are mentioned in Table 1. Further, to realize the NC effect in FinFET, the FEPolarization model is incorporated into the simulation setup. The L-K parameters are well-calibrated against the experimental MFIM (metal-ferroelectric-insulator–metal) capacitor [12], as shown in Fig. 2(c). We assumed uniform polarization in our analysis, considering the homogeneous monodomain thin FE layer for quasi-static analysis. Therefore, the minimum possible permissible value of domain interaction coefficients (g) and damping constant (ρ) provided in TCAD has been selected to resemble our assumptions. The extracted α, β, γ parameters are used to get a good fit of the S-curve (Fig. 2c). The realized NC FinFET show improved performances (Fig. 2d-e), i.e., I_{ON} & SS, due to the internal voltage amplification of the FE-layer.

Table 1

Parameter table.

Parameter	Value
Gate Length (L_G)	20 nm
Fin Height (F_h)	26 nm
EOT	0.9 nm
Spacer Length (L_{SP})	8 nm
Fin Width (F_w)	6.5 nm
Source Doping (N_S)	10^{20} cm^{-3}
Channel Doping (N_C)	10^{16} cm^{-3}

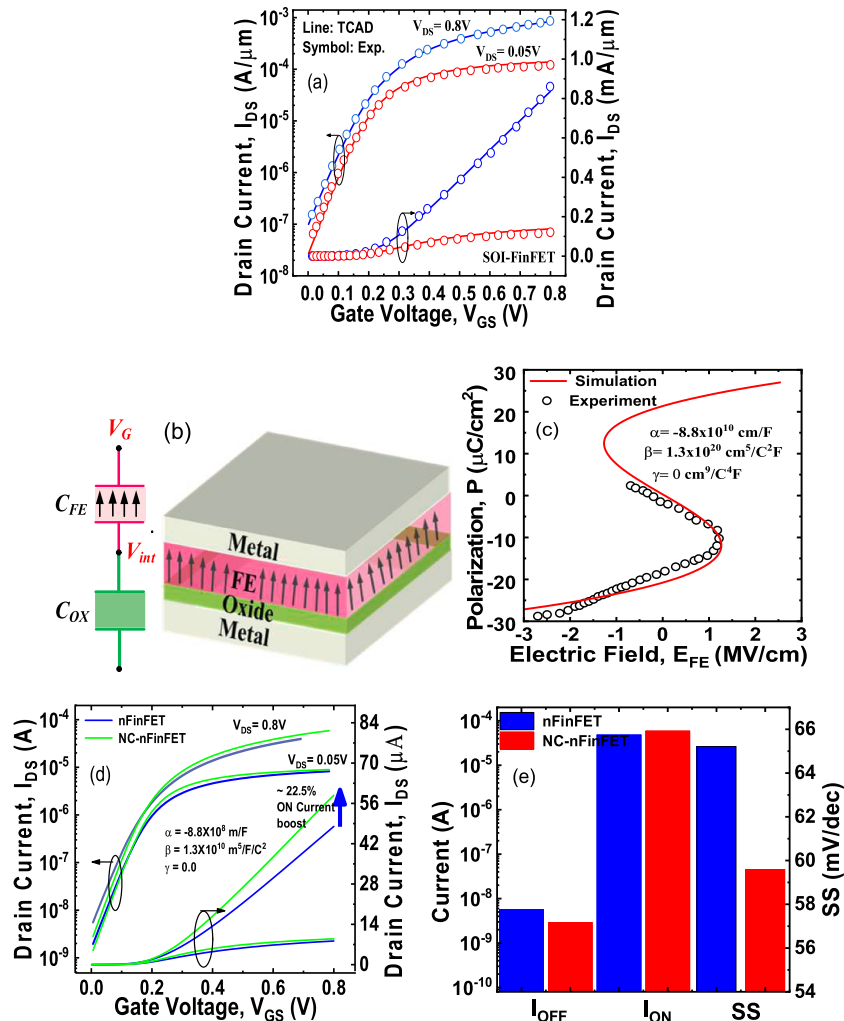


Fig. 2. (a) shows the calibration of the simulated I_{DS} - V_{GS} curves against the experimental data [11]; (b) a schematic of the MFIM capacitor and equivalent capacitor network at the gate stack; (c) shows the calibration of the S-curve against experimental data [12]; (d-e) the realized NC-FinFET (Fig. 1) offers higher I_{ON} , lower I_{OFF} , and steeper SS. The device parameters used in the simulation are mentioned in Table 1.

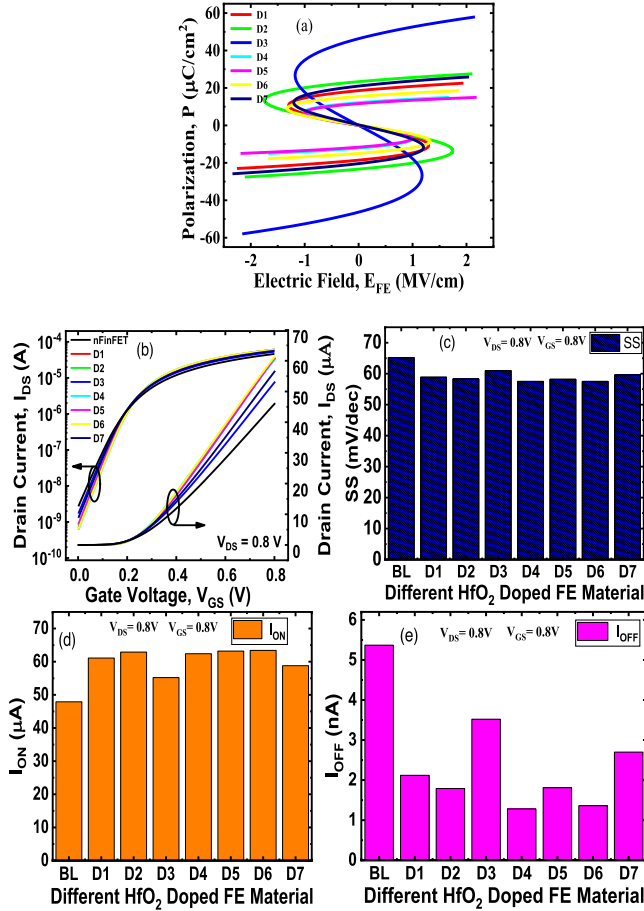


Fig. 3. (a) shows the NC-state is strongly dependent on α_x and β_x , resulting in different S-curves for different α_x and β_x values, as mentioned in Table 2; (b) shows the I_{DS} - V_{GS} characteristics for different material-specific dopants; (c) the SS for different dopants; (d-e) I_{ON} (I_{OFF}) dominantly governed by α_x (β_x).

3. Results and discussion

The paper presents a detailed analysis of HfO_2 dopant-specific parameter-dependent NC FinFET using TCAD and the impact of ambient temperature on Landau parameters in the following subsections:

3.1. L-K parameters for material specific dopants in HfO_2 -based FE layer

In TCAD simulations, the NC effect can be included using the FE polarization model with appropriate Landau parameters, which are dependent on the dopants of the HfO_2 -based FE layer. The different parameters used in our simulation are based on governing Landau-Khalatnikov (L-K) equation, given as:

$$E_{FE} = 2\alpha_x P + 4\beta_x P^3 + 6\gamma_x P^5 + \rho_x \frac{\partial P}{\partial t} - 2g_x \Delta P \quad (1)$$

where P is polarization and E_{FE} is the field across the FE layer. Here, $\alpha_x = -\alpha'_x \times 10^{10} \text{ cm}^5/\text{F}$ and $\beta_x = \beta'_x \times 10^{20} \text{ cm}^5/\text{F} / \text{C}^2$. The default value of $\rho_x = 2.25 \times 10^4 \text{ } \Omega\text{-cm}$, $\gamma_x = 0$, and $g_x = 10^{-4} \text{ cm}^3/\text{F}$ have been considered, as mentioned in the TCAD manual under quasi-static analysis for single domain FE-layer.

Therefore, the vital parameters are α and β , which significantly influence the NC state. For different dopants, we plotted the S-curves, showing the NC regime (Fig. 3a). D₂ offers a larger span of the NC region; however, D₃ shows a higher NC. Whereas the I_{OFF} degrades in D₃

Table 2
Different NC coefficient values for various dopants.

Parameter	α'_x	β'_x
Al (D ₁)	10.55	2.06
Gd (D ₂)	11.36	1.42
La (D ₃)	3.46	0.8
Si (D ₄)	12.99	6.49
Sr (D ₅)	11.29	1.06
Y (D ₆)	12.5	3.28
Zr (D ₇)	8.6	1.3

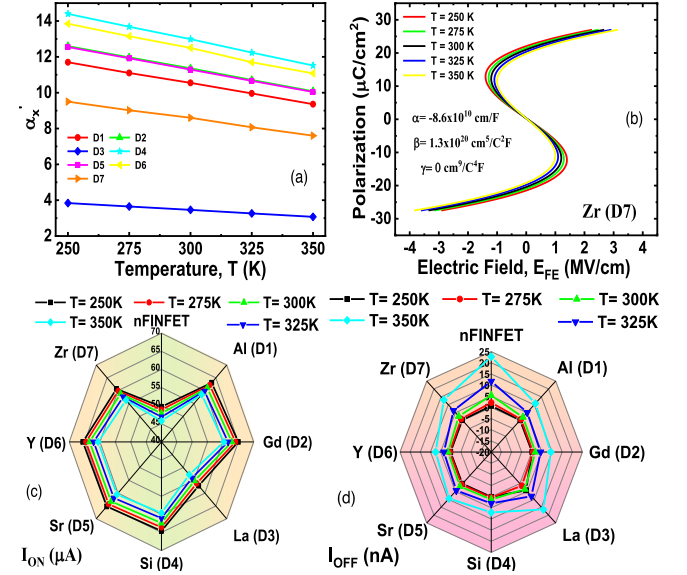


Fig. 4. (a) Shows the impact of temperature on α'_x , in turn, alters the FE polarization; (b) the S-curve with varying temperature influences the NC-state operation; (c-d) the impact of temperature on I_{ON} and I_{OFF} of various dopant-specific FE layers.

due to the lower value of β , in turn, higher SS (Fig. 3c, e). In contrast, the enhanced I_{ON} is achieved in D₄ and D₆, showing a higher dependency of I_{ON} on α (Fig. 3b, d & Table 2).

3.2. Impact of temperature on L-K parameters

The impact of temperature (T) is severe on α , as it is a linear function of T (Fig. 4a), however, β_x and γ_x are weak function of temperature. Mathematically, the impact of temperature variation on α is given as:

$$\alpha_{xT} = \alpha_{0x}(T - T_c) \quad (2)$$

where, α_{0x} has a positive temperature coefficient, and T_c is the Curie temperature (<650 K) above which FE property may be lost. The increase in T reduces the coefficient α_{0x} (Fig. 4a), resulting in a change in α_{xT} (x: dopant). Therefore, the NC regime gets shrinks (Fig. 4b). The I_{ON} thus reduces with higher T (Fig. 4c). An increase in T also causes mobility degradation and the bandgap narrowing; in turn, I_{OFF} increases (Fig. 4d) [13].

3.3. Impact of temperature on g_m

The impact of temperature and Landau parameters are essential for analog design metrics like transconductance (g_m), total gate capacitance (C_{gg}), etc. [14].

As we increase the T, the g_m of the doped HfO_2 -based NC FinFET will decrease (Fig. 5a-e), which causes severe degradation in the device performance. Thus, the impact of α on threshold voltage (V_{th}) is more

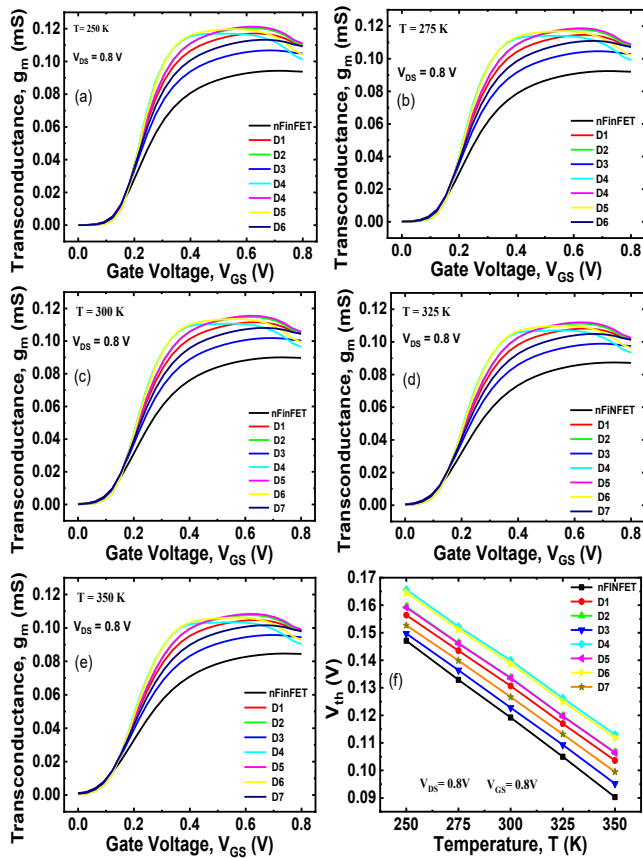


Fig. 5. Shows the impact of increasing the ambient temperature from 250 K to 350 K on (a-e) transconductance (g_m), which is indeed a key parameter in analog circuit design. Increasing the temperature decreases the maximum g_m value due to the deterioration of the dominant ‘ α ’, the Landau parameter. However, the temperature-induced g_m and threshold voltage (V_{th}) deterioration (f) are mitigated by internal voltage amplification provided by the dopant-dependent HfO₂-based FE layer.

pronounced (Fig. 5f).

3.4. C-V characteristics for different dopants

The capacitance matching with varying Landau parameters and temperature is investigated in Fig. 6. The capacitance matching occurs at the subthreshold region for the dopants with higher P_r , i.e., lower α and β . However, the capacitance matching in the saturation region dominates for the dopants with lower P_r values, i.e., higher α and β . Further, the temperature influences the capacitance matching in NC FinFET, resulting in the modulation of channel capacitances (Fig. 6a-e).

4. Conclusions

For a reliable TCAD simulation of the Negative Capacitance (NC) devices, the selection of the appropriate Landau parameters ($\alpha, \beta, \gamma, \rho, g$) is crucial as it frames the span and slope of the S-curve, which states the NC operation. In scaled NC devices, the HfO₂ layer is doped with the appropriate dopants to achieve ferroelectricity. The type of the dopants alters the Landau parameters and, thus, the reliability of the simulated NC devices. For quasi-static operation under consideration of a single domain FE layer, only the α and β parameters play a significant role. The I_{ON} and I_{OFF} are functionally dependent on α and β , respectively. Further, the temperature shows a linear trend with α and strongly influences α_0 (i.e., temperature coefficient). Thus, an increase in temperature deteriorates the device’s performance. Hence, a thorough investigation of

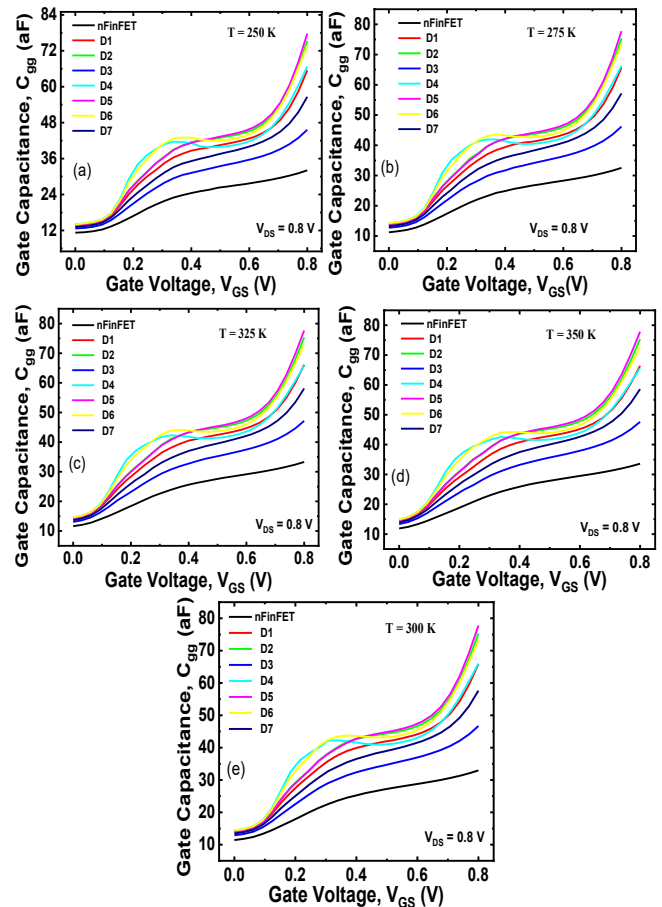


Fig. 6. (a-e) shows the C-V characteristics showing the capacitance matching for different dopants and varying temperatures. The higher (lower) P_r exhibit capacitance matching in the subthreshold (saturation) region.

($\alpha, \beta, \gamma, \rho, g$) is essential to simulate an NC device in TCAD.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The authors do not have permission to share data.

Acknowledgments

N. Bagga greatly acknowledged the support received from the PDM IIIITDM Jabalpur, project title, “Design and Performance Investigation of Negative Capacitance Tunnel FET for Digital/Analog Applications,” project no. IIIITDMJ/ODRSPC/2022/88.

References

- [1] Wu S-Y, et al., “A 7nm CMOS platform technology featuring 4th generation FinFET transistors with a 0.027 μm^2 high density 6-T SRAM cell for mobile SoC applications,” 2016; 2.6.1-2.6.4; *IEEE International Electron Devices Meeting (IEDM)*. doi: 10.1109/IEDM.2016.7838333.
- [2] Rathore S, Jaisawal RK, Suryavanshi P, Kondekar PN. Investigation of ambient temperature and thermal contact resistance induced self-heating effects in nanosheet FET. *Semiconductor Sci Technol* 2022;37:055019. <https://doi.org/10.1088/1361-6641/ac62fb>.

- [3] Jaisawal RK, Rathore S, Kondekar PN, Yadav S, Awadhiya B, Upadhyay P, Bagga N. Assessing the analog/RF and linearity performances of FinFET using high threshold voltage techniques. *Semiconductor Sci Technol* 2022;37:055010. <https://doi.org/10.1088/1361-6641/ac6128>.
- [4] Salahuddin S, Datta S. Use of negative capacitance to provide voltage amplification for low power nanoscale devices. *Nano Lett* 2008;8:405–10. <https://doi.org/10.1021/nl071804g>.
- [5] Chauhan N, Bagga N, Banchhor S, Datta A, Dasgupta S, Bulusu A. Negative-to-positive differential resistance transition in ferroelectric FET: physical insight and utilization in analog circuits. *IEEE Trans Ultrason Ferroelectr Freq Control* 2022;69(1):430–7. <https://doi.org/10.1109/TUFFC.2021.3116897>.
- [6] Jaisawal RK, Rathore S, Gandhi N, Kondekar PN, Bagga N. Role of temperature on linearity and analog/RF performance merits of a negative capacitance FinFET. *Semicond Sci Technol* 2022;37(11):115003.
- [7] Bagga N, Ni K, Chauhan N, Prakash O, Hu XS, Amrouch H. “Cleaved-Gate Ferroelectric FET for Reliable Multi-Level Cell Storage,” 2022; P5-1-P5-5; *IEEE International Reliability Physics Symposium (IRPS)*. doi: 10.1109/IRPS48227.2022.9764553.
- [8] Böscke T, Müller J, Braeuhaus D, Schroeder U, Bottger U. Ferroelectricity in hafnium oxide thin films. *Appl Phys Lett* 2011;99:102903. <https://doi.org/10.1063/1.3634052>.
- [9] Das D, Khan AI. Ferroelectricity in CMOS-compatible hafnium oxides: reviving the ferroelectric field-effect transistor technology. *IEEE Nanotechnol Mag* 2021;15(5): 20–32. <https://doi.org/10.1109/MNANO.2021.3098218>.
- [10] Synopsys TCAD, “Sentaurus Device User Guide, Mountain View CA,” 2021; Synopsys, Inc.
- [11] Lin C-H, Greene B, Narasimha S, Cai J, Bryant A, Radens C, et al., “High performance 14nm SOI FinFET CMOS technology with $0.0174\mu\text{m}^2$ embedded DRAM and 15 levels of Cu metallization,” 2014;3.8.1-3.8.3, *IEEE International Electron Devices Meeting*. doi: 10.1109/IEDM.2014.7046977.
- [12] Hoffmann M, Max B, Mittmann T, Schroeder U, Slesazek S, Mikolajick T. “Demonstration of High-speed Hysteresis-free Negative Capacitance in Ferroelectric $\text{Hf}_0.5\text{Zr}_{0.5}\text{O}_2$ ” 2018; 31.6.1-31.6.4; *IEEE International Electron Devices Meeting (IEDM)*, doi: 10.1109/IEDM.2018.8614677.
- [13] Rathore S, Jaisawal RK, Kondekar PN, Bagga N. Design Optimization of Three-Stacked Nanosheet FET from Self-Heating Effects Perspective, 2022; *IEEE Transactions on Device and Materials Reliability*, doi: 10.1109/TDMR.2022.3181672.
- [14] Banchhor S, Kumar KD, Dwivedi A, Anand B. A new aspect of saturation phenomenon in FinFETs and its implication on analog circuits. *IEEE Trans Electron Devices* 2019;66(7):2863–8. <https://doi.org/10.1109/TED.2019.2914867>.