Analog/RF and Linearity Performance Assessment of a Negative Capacitance FinFET Using High Threshold Voltage Techniques

Rajeewa Kumar Jaisawal, *Member, IEEE*, Sunil Rathore, P. N. Kondekar, and Navjeet Bagga, *Senior Member, IEEE*

***Abstract*—The continued exploration of the ferroelectric-based negative capacitance field effect transistor (NCFET) for energy-efficient and higher current drivability merits has called for an investigation of the device compatibility for analog/RF applications. In this article, we assessed the analog/RF and linearity performance of NC-FinFET by employing high threshold voltage (HVT) techniques. Such techniques are essential to suppress the leakage current and improve the performance in scaled devices. Using well-calibrated TCAD models, we present insight into the advent of incorporating three different HVT approaches: 1) increase in the channel doping ($N_{ch'}$), 2) drain underlap architecture (L_{dsu}), and 3) increase in the channel length ($L_{g'}$) to investigate the analog/RF behavior. Further, various linearity figure-of-merits (FoMs) has been examined using g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3, IMD_3, and 1-dB compression point. We also varied $N_{ch'}$, L_{dsu}, and $L_{g'}$ to optimize the proposed HVT techniques for optimum performance. Moreover, the Gummel symmetry test, as a linearity measure, has been done for the optimized HVT-NCFinFET to investigate the drain current symmetry. Thus, the obtained results serve as a design guideline for adopting the NC-FinFET pertaining to low-power RF applications.**

***Index Terms*—Negative capacitance, FinFET, high threshold voltage (HVT), analog/RF, linearity, gummel symmetry.**

I. Introduction

IN THE last few decades, FinFET has gained significant attention due to improved gate electrostatic and superior scalability. Still, the research (the simulation cum modeling and fabrication) on sub-14nm FinFET governs a broad scope of memory, RF, and switching applications [1], [2], [3], [4], [5]. Following the emerging trend, the ferroelectric (FE) based Negative Capacitance (NC) FETs have established themselves as a staunch promising candidate for higher drivability and steeper subthreshold slope (SS) with their outstanding energy-efficient performance compared to conventional CMOS devices. An NC-FinFET can be realized by placing a FE layer in the gate stack of the baseline FinFET. The NC effect induces internal voltage amplification, which raises the surface potential, thus, the ON current. NC-based devices also possess some unique behavior, such as drain-induced barrier rising (DIBR), negative differential resistance (NDR), and provide steep switching, i.e., sub-60 mV/decade SS at room temperature (300 K) [6], [7], [8], [9], [10], [11]. The most ushered NCFET studies have primarily focused on metal-ferroelectric-metal-insulator-semiconductor (MFMIS) architecture, which is opted for simplicity in understanding and modeling the device [9], [11]. However, the leakage current in the MFMIS configuration makes the biasing difficult due to the instability and multi-domain effect [12], [13]. The reduced efficacy of MFMIS structure can be alleviated by employing a practical designing approach, i.e., metal-ferroelectric-insulator- -semiconductor (MFIS) structure, comprising the spatially varying potential between FE and dielectric interface [14]. The inclusion of CMOS-compatible thin FE material having significantly high remanent polarization (i.e., up to 45 μC/cm^2) and a large coercive electric field ($\sim$1–2 MV/cm) sandwiched between the metal and gate-dielectric of the baseline FinFET reaffirms the hegemony of the NC-FinFET in the circuit applications [13], [15], [16]. The literature is abounding with circuit-level investigations and demonstrations of the improved performance of NC-based circuits such as comparators, current mirrors, sample-and-hold circuits, analog switches, and differential amplifiers clocked at high-frequency analog and digital applications [8], [9], [10]. Despite high performance and better control of short-channel effects (SCEs), it is necessary to thoroughly investigate and optimize the analog/RF merits to make the FinFET technology ideal for ultralow power and high-frequency analog/RF applications. The figure-of-merits (FoMs) such as gate capacitance (C_{gg}), unity gain cut-off frequency (f_T), maximum frequency of oscillation (f_{max}), and transconductance (g_m), etc. are widely opted parameters to investigate the analog/RF behavior [11], [17], [18]. Moreover, the device linearity analysis also requires proper attention, ensuring the minimized higher-order harmonics and intermodulation distortion [19], [20]. Therefore, studying analog/RF and linearity performance of the FinFET is time and application-demanding. In all the stated FoMs, the device's threshold voltage (V_{th}) plays a vital role; thus, it must be modulated per scaled geometries.

In this article, we demonstrated the high-threshold voltage (HVT) techniques in NC-FinFET to enhance the overall device characteristics over its baseline counterpart, i.e., low threshold voltage (LVT-NCFinFET). ***Key Contributions of this work:*** Using well-calibrated TCAD models, we investigated: (*i*) the

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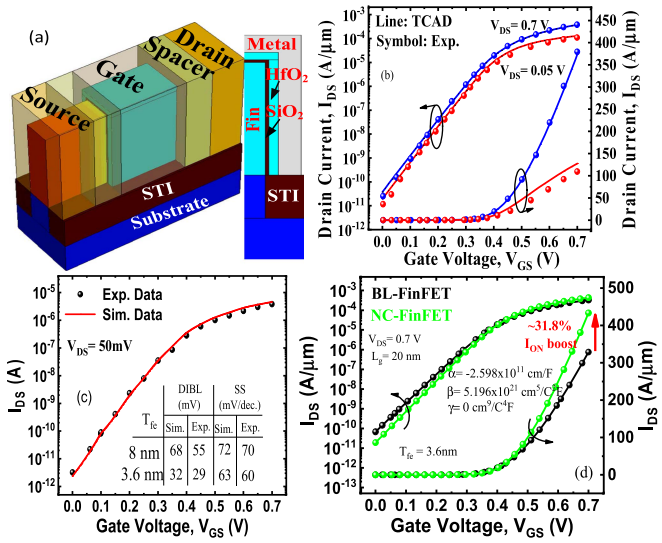

Fig. 1. (a) 3D schematic of the NC-FinFET simulated using TCAD, which is realized by replacing the conventional high-k layer of the BL-FinFET with a doped HfO_2, i.e., $Hf_{0.5}Zr_{0.5}O_2$ layer; (b) calibration of the transfer characteristics (I_{DS}–V_{GS}) of the baseline FinFET against the experimental data [5]; (c) calibration of the transfer characteristics against the experimental data of the NC-FinFET for FE thickness 8nm. The inset shows the data extracted for FE thickness 3.6nm; (d) demonstration of current amplification in I_{DS}-V_{GS} characteristics by incorporating the NC effect. The Landau parameters are explicitly mentioned.

impact of employing three different HVT techniques on the performance of MFIS-based NC-FinFET; (*ii*) the analog/RF performance of HVT-NCFinFET is based on performance metrics such as g_m, C_{gg}, f_T, gain-bandwidth product, and transconductance-frequency product, etc.; (*iii*) different FoMs such as g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3, IMD_3, and 1-dB compression points to analyze the linearity of HVT-NCFinFETs over its LVT counterpart; (*iv*) the optimum proposed HVT technique and also perform a fair comparison of analog/RF and linearity performance of the optimized HVT techniques with baseline LVT-NCFinFET; *(v)* Gummel symmetry test (GST) employed as a measure of linearity to check the drain current symmetry and continuity.

II. Device Structure and Simulation Setup

In this work, we realized NC-FinFET using *Sentaurus* TCAD [21] using a 14 nm industry-standard baseline FinFET, as shown in Fig. 1(a). TCAD setup is calibrated adequately against the experimental data [5].

In baseline FinFET, the gate-stack of equivalent oxide thickness (EOT) equals 0.9 nm is considered. Si_3N_4 spacer is used as a spacer to suppress the fringing capacitances by minimizing the interference of the additional outer drain electric field towards the active channel region. Uniform doping is employed in the source/drain (S/D) and the channel region. In contrast, the recessed S/D is doped with Gaussian doping to minimize the random dopant fluctuations (RDF) and reduce the external resistance by realizing the realistic scenario. The drain current of FinFET is normalized by effective channel width ($W_{eff} = 2F_h+F_w$). TCAD setup incorporates physics models such as SRH and Auger models for carrier generation and recombination. The quantum-potential and the drift-diffusion models

TABLE I
Parameter Table

Parameters	Value	Parameters	Value
Gate length (L_g)	20 nm	Channel doping (N_{ch})	1×10^{16} cm^{-3}
Fin height (F_h)	42 nm	Source/ Drain doping ($N_{S/D}$)	1×10^{20} cm^{-3}
Fin width (F_w)	8 nm	Substrate doping (N_{SUB})	5×10^{17} cm^{-3}
Spacer length (L_{SP})	7.5 nm	Si_3N_4 dielectric constant (ϵ_{sp})	$7.5\epsilon_0$
STI thickness (T_{STI})	10 nm	HfO_2 dielectric constant (ϵ_b)	$25\epsilon_0$

render the electrical performance and facilitate carrier transport. The carrier mobility behavior is captured by including the Caughey-Thomas model for high field saturation. Lombardi model to alleviate the mobility degradation due to high-k dielectric [22], the ballistic mobility model to capture the short channel effects, and the doping-dependent (UniBo) model account for lattice scattering and electron-hole scattering [23]. Finally, the metal gate (TiN) work function is tuned to match the simulation results with the experimental data (Fig. 1(b)). Further, to realize the NC-FinFET, the high-k layer in BL-FinFET is replaced by a doped-HfO_2 (i.e., $Hf_{0.5}Zr_{0.5}O_2$) layer, which acts as a FE layer [24]. Over time, the $Hf_{0.5}Zr_{0.5}O_2$ (HZO) has been extensively used as a FE material due to its high scalability and CMOS process compatibility, as the atomic radius of the Zr is almost equal to the Hf, and they have approximately equal lattice parameters and crystal phases [16]. The FEPolarization model is used in TCAD to acquire the requisite negative capacitance characteristics. The ferroelectricity arises due to the unique intrinsic relation of the electric field (E_{fe}) and its polarization (P) of the FE material, which can be modeled by using the Landau-Khalatnikov (LK) expression [11], given as follows:

$$E_{fe} = \frac{V_{fe}}{T_{fe}} = 2\alpha P_S + 4\beta P_S^3 + 6\gamma P_S^5 + \rho\frac{\partial P_S}{\partial t} - 2g\Delta P_S \tag{1}$$

where α, β, and γ are the static FE material-dependent specified Landau constants, ρ is the ferroelectric damping constant, and g is the coupling coefficient. T_{fe} and V_{fe} represent the thickness and the voltage drop across the FE layer, respectively. For smaller V_{fe}, the electric displacement or gate charge density (Q_g) and ferroelectric surface polarization (P) can be expressed by using the boundary condition across the metal-ferroelectric interface as:

$$Q_g = P_S + \varepsilon_0\varepsilon_b E_{fe} \approx P \tag{2}$$

Sentaurus TCAD self-consistently solves the electrostatic of the Poisson equation and the single domain LK equation (by combining (1) and (2) to obtain the voltage across the ferroelectric material as a function of the gate charge density). The value of static Landau coefficients: $\alpha = -2.598\times10^{11}$ cm/F, $\beta = 5.196\times10^{21}$cm^5/F/C^2 and $\gamma = 0$ cm^9/F/C^4 are extracted by fitting the experimental data of the NC-FinFET. Moreover, the thickness and permittivity of the HfO_2 layer are considered in the permissible range to obtain a hysteresis-free NC operation calibrated against the experimental data (Fig. 1(c)). Table I articulates the device parameters used in the simulation to get a proper calibration.

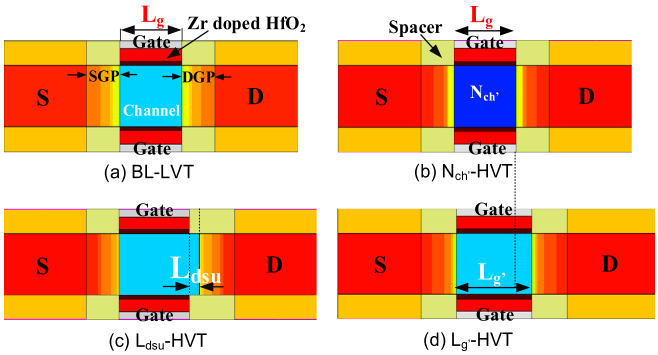

Fig. 2. 2D schematic of (a) conventional LVT-NCFinFET (L_g = 20nm), (b) HVT-NCFinFET with increased channel doping ($N_{ch'} = 2\times 10^{18}$ cm^{-3}); (c) HVT-NCFinFET with drain-side underlap (L_{dsu} = 4nm); and (d) HVT-NCFinFET with increased gate length ($L_{g'}$ = 24nm). Here SGP (DGP) shows the S/D side extension region with Gaussian doping.

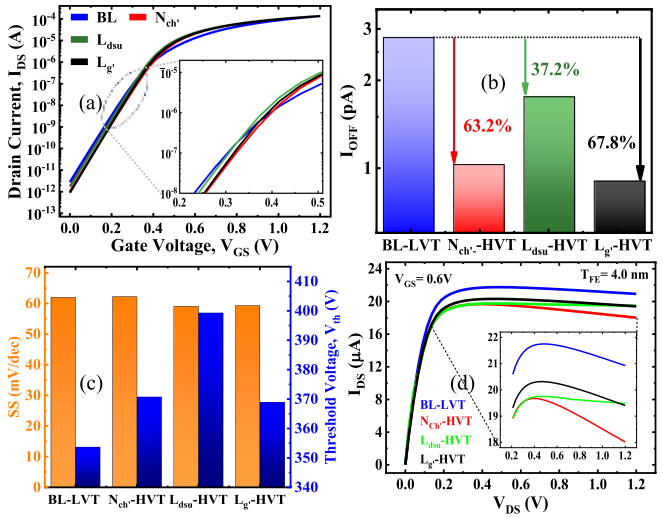

Fig. 3. Impact of $N_{ch'}$, L_{dsu}, and $L_{g'}$ HVT techniques on (a) leakage current illustrated by the transfer characteristics (I_{DS}–V_{GS}) with maintaining iso-ON current for a fixed V_{DS}. $L_{g'}$ HVT is found as the most effective technique to suppress the I_{OFF}; (b) percentage improvement of leakage current, i.e., I_{OFF}; (c) SS and V_{th} are extracted for all the HVT techniques, i.e., N'_{ch}, L_{dsu}, and L'_g; and (d) demonstration of negative drain resistance (NDR) on output characteristics. L_{dsu}-HVT exhibits resilience against the NDR effect.

We assumed uniform polarization in our analysis owing to the homogeneous monodomain of thin-layer FE material. Therefore, the minimum permissible value of domain interaction coefficients (g) provided in TCAD has been selected to resemble our assumptions. We have taken the default values of the damping coefficient ($\rho = 2.25\times 10^4$ Ω-cm) and coupling coefficient (g = 1×10^{-4} cm^3/F) in our simulation. The impact of incorporating the FE layer in the BL-FinFET to realize NC-FinFET can be depicted in the transfer characteristics, as shown in Fig. 1(d). The NC-FinFET provides ∼31.8% improvement in I_{ON} and improved SS (∼19.2% improvement over the baseline) due to the internal voltage amplification obtained using NC operation.

III. Results and Discussion

In this section, we discussed the impact of including three different HVT techniques on NC-FinFET over baseline FinFET by investigating the leakage current, analog/RF, and linearity merits. Fig. 2 shows the two-dimensional schematic of all the HVT techniques and the conventional low threshold voltage (LVT) NC-FinFET architectures. The three high threshold voltage (HVT) NC-FinFETs architectures are: (*i*) HVT due to increasing channel doping concentration (N'_{ch}) [Fig. 2(b)]; (*ii*) HVT due to drain-side underlap (L_{dsu} = 4 nm) [Fig. 2(c)], and (*iii*) HVT due to increased gate length (L'_g = 24 nm) [Fig. 2(d)]. We have considered V_{DS} = 0.7V in all subsequent analyses unless stated otherwise. Our simulation has not considered higher V_{DS} conditions to avoid drain coupling effect in FE polarization [7].

A. Subthreshold Behavior and NDR Analysis

Devices with multiple threshold voltages (V_{th}) are frequently needed for power-efficiency optimization [25]. HVT-NCFinFETs have the advantage of optimized power performance over LVT-NCFinFET. Among numerous HVT techniques, one of the possible/simpler ways to get a higher threshold voltage (V_{th}) is by increasing the channel doping concentration (N'_{ch}). However, in the static random-access memory (SRAM), gate-S/D underlap devices are used to alter the V_{th} and improve I_{OFF} and stability [26]. In microprocessor design, increasing gate length (L'_g) is utilized [27] as an HVT technique. Fig. 3(a) comprehensively describes the significant improvement in leakage current after incorporating different HVT techniques (i.e., N'_{ch}, L_{dsu}, or L'_g) on the I_{DS}-V_{GS} characteristics over the LVT-NCFinFET. With the adoption of N'_{ch}-HVT, L_{dsu}-HVT, and L'_g-HVT, the leakage current of LVT-NCFinFET improves by 63.2%, 37.2%, and 67.8%, respectively (Fig. 3(b)). Therefore, by using the HVT techniques, the drain current improves significantly in the subthreshold region, explaining that high V_{GS} is required to turn on the HVT-NCFinFETs. Fig. 3(c) describes the effect of different HVT techniques on the SS and V_{th} of different NC-FinFETs. The V_{th} of HVT-NCFinFETs has been improved by ∼4.8%, 12.86%, and 4.29%, respectively, for N'_{ch}-HVT, L_{dsu}-HVT, and L'_g-HVT configurations. We employed a classical approach of the constant current method to calculate the V_{th} [28]. The SS of L_{dsu} and L'_g HVT-NCFinFETs improved by ∼4.7% compared to LVT-NCFinFET. Fig. 3(d) shows output characteristics (I_{DS}-V_{DS}) exhibiting the negative differential resistance (NDR) due to the dominance of drain coupling capacitance over the FE capacitance-induced amplification factor. The L_{dsu}-HVT shows a weaker NDR effect owing to the reduced drain electric field, in turn, the drain coupling capacitance [7], [9].

B. Analog/RF Analysis

This subsection describes the impact of HVT techniques on the analog/RF performance of NC-FinFETs. The vital device parameters such as g_m, f_T, C_{gg}, transconductance frequency product (TFP), and gain-bandwidth product (GBP) have been investigated and compared with the LVT-NCFinFET. Out of state above, the g_m (i.e., $\partial I_D/\partial V_{GS}$) is a critical analog/RF parameter, defined as the variation in drain current by varying the gate voltage (V_{GS}) at a fixed V_{DS}. The g_m demarcates the gain of the analog circuit, and a higher value is necessary for the improved analog performance of the NC-FinFET-based circuits [29]. In general, g_m is a vital function of the carrier mobility (μ), total gate capacitance (C_{gg}), device geometrical parameters (W/L), and the overdrive voltage, i.e., (V_{GS} - V_{th}). The plot

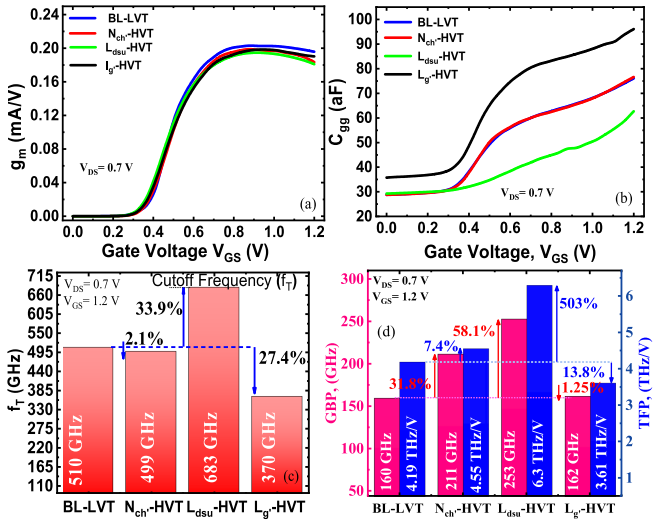

Fig. 4. Impact of incorporating various HVT techniques on (a) g_m; (b) C_{gg}; (c) f_T; (d) GBP and TFP of the LVT-NCFinFET and HVT-NCFinFETs.

of g_m with varying V_{GS} will increase till a certain value of the V_{GS} as the device would be on weak inversion. The peak value of g_m is obtained around $V_{GS} = 0.6$V. However, with a further increase in V_{GS}, the surface potential gets pinned, the NC-FinFET device strongly inverts the channel, and the device enters the linear region.

Thus, the inversion charge density does not profoundly modulate with V_{GS}, i.e., $\partial I_D/\partial V_{GS}$ decreases as the drain current gets saturated. In this case, the conduction current is primarily due to drift; thus, the peak value of g_m starts decreasing and becomes a function of V_{DS}. The proposed work analyses the impact of the overdrive voltage on the NC-FinFET by explicitly modulating the V_{th} using the HVT techniques while keeping the remaining parameters constant. Fig. 4(a) shows the g_m variation with varying V_{GS} for LVT and HVT-NCFinFETs. The peak value of g_m decreases by ∼2.36%, 3.9%, and 2.12% for Nch′, Ldsu, and Lg′ HVT-NCFinFET, respectively, when compared to LVT-NCFinFET, due to an increase in the value of the V_{th} which implicitly decreases the value of overdrive voltage. The HVT techniques have an appreciably higher impact on C_{gg} of the NC-FinFET, comprising the oxide capacitance, ferroelectric capacitance, and spacer-induced fringing capacitance. C_{gg} increases with the applied V_{GS}, as shown in Fig. 4(b). The L_{dsu} HVT-NCFiNFET has a smaller C_{gg} due to the reduced spacer-induced fringing capacitance. Fig. 4(c) and (d) depicts the analog/RF merits regarding f_T, f_{max}, GBP, and TFP.

The frequency at which the current/voltage gain (power gain) of the transistor becomes unity is defined as f_T (f_{MAX}), given as [20].

$$f_T \approx \frac{g_m}{2\pi C_{gg}} \tag{3}$$

$$f_{max} \approx \frac{f_T}{2\sqrt{g_{ds}\ (R_g + R_s) + 2\pi f_T R_g C_{gg}}} \tag{4}$$

where C_{gg} is the total gate capacitance defined as $C_{gg} = C_{gd} + C_{gs} + C_{parasitic}$. C_{gd} is gate-to-drain capacitance, C_{gs} is gate-to-source capacitance, and $C_{parasitic}$ is parasitic capacitance. The source resistance is $Rs = 0.5R_g$ (here, R_g is the gate resistance), and in general, the $Rs = 50\,\Omega$ opts for most of the RF applications [19]. Mixed-mode transient TCAD simulations have been used to extract the capacitances using 1MHz as a default signal frequency [30]. Fig. 4(c) shows that the peak value of f_T is increased by ∼33.9% for L_{dsu}-HVT NCFinFET; however, it diminished by 2.1% and 27.4% for $N_{ch'}$-HVT and L'_g-HVT NCFinFETs, respectively, when compared to LVT-NCFinFET. Equation (3) defines the overall impact of g_m and C_{gg} on f_T; therefore, the resultant change in these two parameters will determine the effective change in f_T. The smaller C_{gg} results in higher f_T for L_{dsu}-HVT NCFinFET. The GBP and TFP are given as:

$$GBP = \frac{g_m}{2\pi 10 C_{gd}} \tag{5}$$

$$TFP = \left(\frac{g_m}{I_{DS}}\right) f_T \tag{6}$$

Fig. 4(d) shows the GBP and TFP of the HVT-NCFinFETs compared to LVT-NCFinFET. The GBP of L_{dsu}-HVT and L'_g-HVT NCFinFET is enhanced by 31.8% and 58.1%, respectively; however, for Nch′-HVT, it deteriorates by 1.25% when compared to LVT-NCFinFET due to significant dominance of C_{gd} over g_m. The TFP (6) specifies the possible gain per unit power dissipation in the NC-FinFET analog/RF FoM, and high values are required for analog/RF efficient low-power RF applications. The TFP of L_{dsu}-HVT and N'_{ch}-HVT NCFinFET increases by ∼50.3% and 7.4%; however, for L'_g-HVT NC-FinFET, it decreases by 13.8%, Fig. 4(d). This is due to the strong dependence on f_T. Thus, including HVT techniques improves the analog/RF performance over LVT-NCFinFET with an appreciable improvement in the leakage current.

C. Linearity Performance and Distortion Analysis

This subsection discusses the extensive linearity analysis and harmonic distortion characteristics of LVT-NCFinFET and HVT-NCFinFETs. The devices must have the least degree of harmonic distortion to save power in an RF communication system. The different FoMs, such as higher-order harmonics transconductance (g_{m2}, g_{m3}), interpolated input voltage (VIP_2, VIP_3), input power extrapolated point (IIP_3), extrapolated intermodulation distortion power (IMD_3), and 1-dB compression point, etc. have been investigated to assess the distortion and linearity performance of NC-FinFET. The g_{m2} and g_{m3} contribute to major disturbances in any communication system and need proper attention, given as follow:

$$g_{mn} = \frac{\partial^n I_{DS}}{n! \partial V_{GS}^n} \tag{7}$$

where n = 1, 2 shows the second and third order of g_m, i.e., g_{m2} and g_{m3}. Fig. 5(a) and (b) depicts the variation of g_{m2} and g_{m3} of HVT-NCFinFETs and LVT-NCFinFET with varying V_{GS}. The peak value of g_{m2} and g_{m3} should be lower, and the zero-crossover point (ZCP) of g_{m2} should occur at lower V_{GS} for better linearity performance. The V_{GS} value where g_{m2} crosses the zero axis for the first time is defined as ZCP and will determine the DC bias point for the optimum device operation. The value of g_{m2} and g_{m3} are lower for HVT-NCFinFETs at lower V_{GS} and decrease sharply at higher V_{GS}, indicating the improvement in the linearity performance. VIP_2 and VIP_3 are also essential metrics for measuring linearity and distortion characteristics. To design a device for better linearity performance

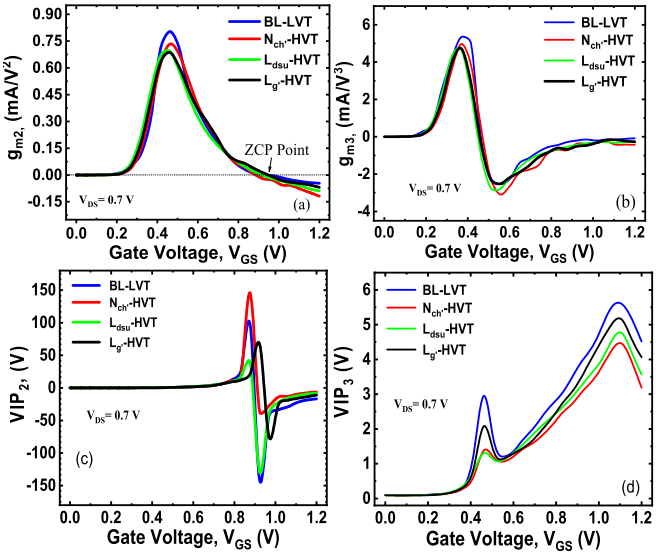

Fig. 5. The impact of different HVT techniques on (a) second-order transconductance harmonics (i.e., g_{m2}); (b) third-order transconductance harmonics (i.e., g_{m3}); (c) VIP_2; and (d) VIP_3 of NC-FinFET as a function of V_{GS}.

with less distortion, the values of VIP_2 and VIP_3 should be maximum [19]. The interpolated input voltage where first-order harmonic voltage is identical to second-order and third-order harmonics voltage is defined as VIP_2 and VIP_3, respectively.

The VIP_2 and VIP_3 can be calculated as [19], [20]:

$$VIP_2 = 4 \times \left(\frac{g_{m1}}{g_{m2}}\right) \tag{8}$$

$$VIP_3 = \sqrt{24 \times \left(\frac{g_{m1}}{g_{m3}}\right)} \tag{9}$$

Fig. 5(c) and (d) shows the variation of VIP_2 and VIP_3 as a function of V_{GS} at constant $V_{DS} = 0.5V$ for HVT- and LVT-NCFinFETs. It is clear that, the peak value of VIP_2 and VIP_3 for HVT-NCFinFETs are higher compared to LVT-NCFinFET due to the suppression of higher-order transconductance harmonics distortion coefficients [Fig. 5(a) and (b)]. Therefore, the linearity performance of HVT-NCFinFETs is enhanced compared to LVT-NCFinFET. Further, IIP_3 and IMD_3 describe the extrapolated input power and intermodulation power when the first-order harmonic power conforms to the third-order power harmonic, respectively, and are given as follows [19], [20]:

$$IIP_3 = \frac{2}{3} \times \left(\frac{g_{m1}}{g_{m3} \times R_s}\right) \tag{10}$$

$$IMD_3 = \left[\frac{9}{2} \times (VIP_3)^2 \times g_{m3}\right]^2 \times R_s \tag{11}$$

Here, $R_S = 50\ \Omega$ has opted for RF application [19]. Fig. 6(a) shows that the value of IIP_3 of NC-FinFET also increases with increasing V_{GS} due to suppressed third-order transconductance harmonics. The IIP_3 of HVT-NCFinFETs is found to be higher over LVT-NCFinFET, revealing the improvement in the linearity performance. In the wireless communication system, IMD_3 is used to measure the nonlinearity in the static characteristics of the device. The suppression of the odd-order harmonics is necessary to enhance the device's linearity against signal distortion because even-order harmonics can be eliminated using the balanced circuit topology. In Fig. 6(b), HVT-NCFinFETs show a lower value of IMD_3 compared to IIP_3 (Fig. 6(a)) value at lower V_{GS}, ensuring that in the HVT-NCFinFETs, the hot carrier effects have been subsided. Therefore, the device's power and distortion reduces. The 1-dB compression point determines the linearity's upper limit and signifies the power level where the gain is reduced by 1-dB from its small-signal input value [19], [20] and expressed as:

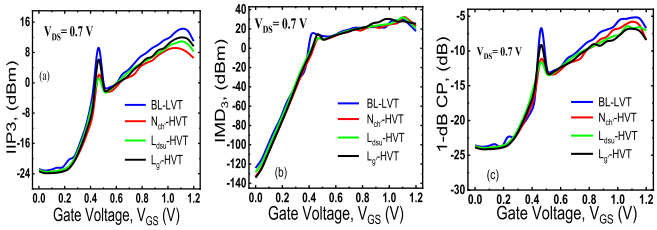

Fig. 6. Impact of HVT techniques on (a) IIP_3, (b) IMD_3, and (c) 1-dB compression point (CP) as a function of V_{GS}.

TABLE II
COMPREHENSIVE ANALYSIS OF ANALOG/RF AND LINEARITY PERFORMANCE PARAMETERS OF NC-FINFET

Parameter	BL-LVT	N_{ch}-HVT	L_{dsu}-HVT	L_g-HVT
I_{OFF} (pA)	2.9	1.1	1.75	0.8
SS (mV/dec.)	62	62.2	59.07	59.3
V_{th} (mV)	353.8	370.8	399.3	369
I_{ON}/I_{OFF} (10^6)	1.7	3.0	3.8	4.2
C_{gg} (aF)	76	76.6	53.7	52.8
C_{gd} (aF)	34.8	39.2	26.6	25.8
f_T (GHz)	510	499	683	370
GBP (GHz)	160	211	253	162
TFP (THz)	4.19	4.55	6.3	3.61
Linearity Performance FoMs				
g_m (mA/V)	0.261	0.232	0.243	0.237
g_{m2} (mA/V^2)	1.14	0.87	1.07	0.99
g_{m3} (mA/V^3)	6.77	4.67	6.19	5.68
VIP_2 (V)	12.19	2.53	18.13	20.80
VIP_3 (V)	2.41	2.38	2.99	2.09
IIP_3 (dBm)	3.17	4.3	2.9	3.87
IMD_3 (dBm)	26.87	20.77	22.39	23.54
1-dB CP (dB)	-9.64	-9.70	-8.71	-10.26

$$1-dB \text{ compression point} = 0.22\sqrt{\left(\frac{g_{m1}}{g_{m3}}\right)} \tag{12}$$

Fig. 6(c) depicts the variation of the 1-dB CP for LVT and HVT NC-FinFETs, and it is observed that the peak value of 1-dB CP for HVT-NCFinFETs is high compared to LVT-NCFinFET. Thus, the linearity of the HVT-NCFinFETs improves the device's performance and makes it suitable for RF applications. Table II shows a fair comparison of the acquired results obtained for HVT-NCFinFET and compared with LVT-NCFinFET counterparts. Therefore, a proper design guideline is necessary to suppress the leakage current, which is beneficial for designing a low-power RF application.

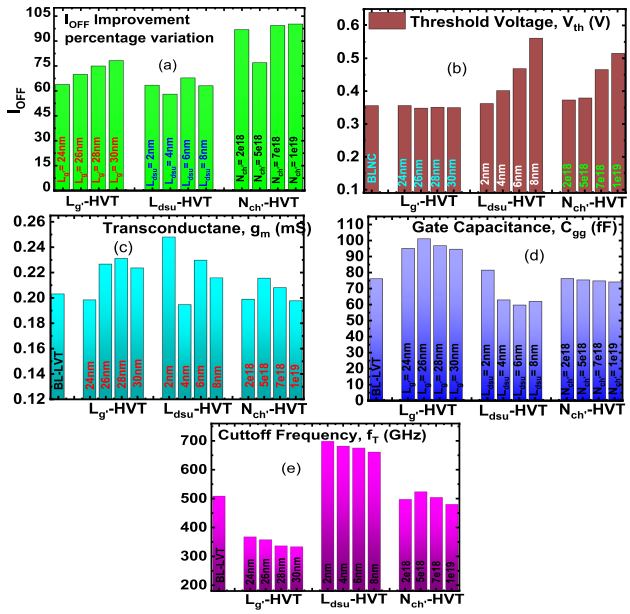

Fig. 7. Analog performance FoMs of the proposed HVT techniques for varying values of $N_{ch'}$, L_{dsu}, and $L_{g'}$ compared to baseline LVT-FinFET: (a) I_{OFF} at iso-I_{ON}, (b) V_{th}, (c) g_m, (d) C_{gg}, and (e) cut-off frequency (f_T).

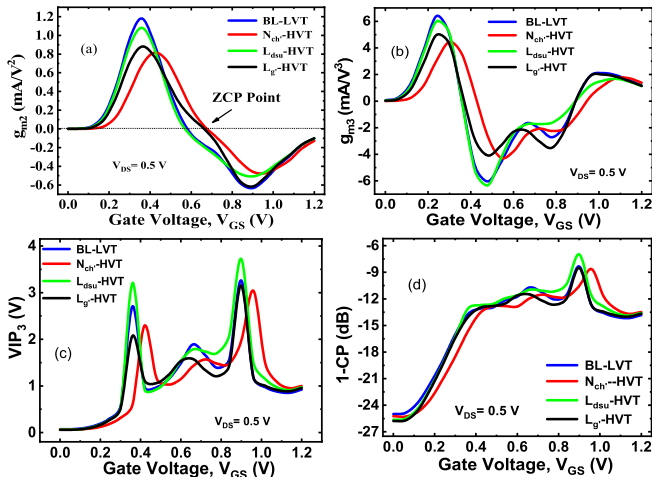

Fig. 8. Linearity metrics for optimized values of $N_{ch'}$, L_{dsu}, and $L_{g'}$ (a) gm_2, (b) gm_3, (c) VIP3, and (d) 1-dB compression point.

D. Device Optimization

We further explored the proposed HVT techniques for varying $N_{ch'}$, L_{dsu}, and $L_{g'}$ values for optimum performances and investigated the impact on analog/RF and linearity characteristics. The trade-off performance parameters are compared with the LVT-NCFinFET. Fig. 7 shows comparative bar charts of parameters such as I_{OFF}, V_{th}, g_m, $C_{gg,}$ and f_T. We optimized the devices for the best leakage current and f_T performances by keeping the iso-I_{ON} condition. Thus, to present a clear distinction between FoMs of HVT and LVT-NCFinFETs, we plotted the second-order derivatives, i.e., g_{m2}, g_{m3}, VIP_2, VIP_3, 1-dB CP, etc., for optimized values of $N_{ch'}$, L_{dsu}, and $L_{g'}$, as shown in Fig. 8. It is clear that increasing the $N_{ch'}$ increases the channel depletion charges and decreases the inversion layer charges, which enhances the V_{th}. Thus, the decrease in overdrive

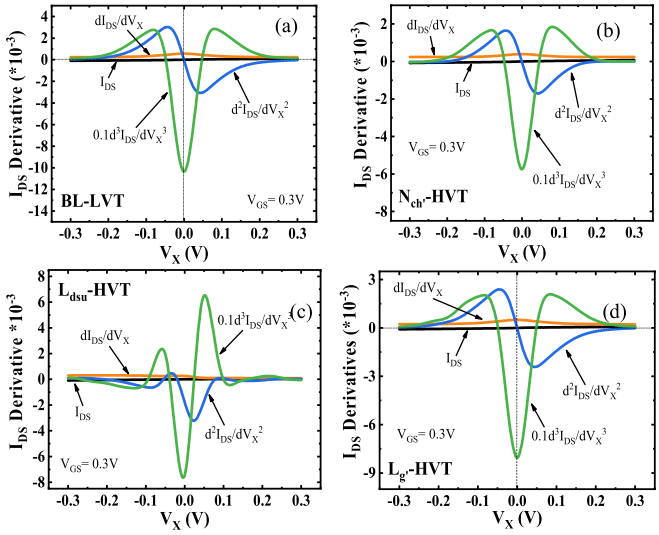

Fig. 9. Plot of drain current and its derivates for the (a) LVT; (b) $N_{ch'}$-HVT; (c) L_{dsu}-HVT; and (d) $L_{g'}$-HVT to investigate the I_{DS} symmetry of the NC-FinFET devices at $V_{GS} = 0.3$ V.

voltage decreases the g_m. Hence the C and f_T decrease for the $N_{ch'}$-HVT NCFinFET.

Moreover, $N_{ch'}$-HVT techniques will provide leakage-current mitigation and increase the threshold voltage variation compared to other HVT techniques. Increasing the channel length ($L_{g'}$) increases the overall oxide capacitance (C_{ox}), which increases the total gate capacitance (C_{gg}) of the $L_{g'}$-HVT technique due to enhanced charge density per unit area. In contrast, by enhancing the drain-side underlap (L_{dsu}) after 4nm, the drain capacitance decreases, which decreases the total gate capacitance. Hence, HVT techniques with $L_{g'} = 28$nm, $L_{dsu} = 4$nm, and $N_{ch'} = 5\times10^{18}\text{cm}^{-3}$ provide the optimum value for analog/RF and linearity performance improvement.

E. Gummel Symmetry Test for the Optimized HVT NC-FinFET

As an additional measure of linearity analysis, the Gummel symmetry test (GST) is performed for the optimized HVT-FinFETs. GST is a testimony of the drain current (I_{DS}) symmetry achieved by biasing the bulk (substrate) to zero and applying an independent voltage source of $2V_x$ across the drain and source terminals [31]. In GST circuit setup, I_{DS} exhibits the odd symmetry with respect to the applied voltage and its higher-order derivates (*i.e.*, $\partial I_x^n/\partial V_x^n$) possess no singularity, i.e., continuous at $V_x = 0$V [32].

Fig. 9(a)–(d) shows the variation of I_{DS} and its derivative variation in the weak inversion regime ($V_{GS} = 0.3$V) for the available HVT-NCFinFETs. All the HVT-NCFinFETs exhibit the I_{DS} symmetry and continuity at $V_x = 0$V except L_{dsu} HVT-NCFinFET, which indicates I_{DS} continuity and asymmetricity for the higher order derivatives due to the existence of spacer-induced fringing capacitance in the drain overlap region. Therefore, the GST is employed as a linearity measure to the proposed HVT NCFinFETs, offering optimized design guidelines.

IV. Conclusion

The crux of the article is to investigate and optimize the analog/RF and linearity performances of the MFIS-based Negative

Capacitance (NC) FinFET using high-threshold voltage (HVT) techniques. Using well-calibrated TCAD models, we realized three different HVT techniques: (*i*) increasing channel doping ($N_{ch'}$-HVT); (*ii*) drain-side underlap modulation (L_{dsu}-HVT); and (*iii*) increasing the channel length ($L_{g'}$-HVT) to investigate the performance metrics of NC-FinFET. The proposal of HVT techniques and their impact on analog/RF and linearity performance has been analyzed through various figure-of-merits such as transconductance, gate capacitance, unity gain cut-off frequency, the maximum frequency of oscillation, interpolated input voltage (i.e., VIP_2, VIP_3), second-order derivatives of transconductance (i.e., g_{m2}, g_{m3}), etc. We observed that $L_{g'}$-HVT NCFinFET shows significant improvement in the leakage current (I_{OFF}) over $N_{ch'}$-HVT and L_{dsu}-HVT due to the reduced DIBL effect. $N_{ch'}$-HVT shows improved second-order derivatives owing to lesser inversion charge density. Moreover, f_T, gain-bandwidth product, and transconductance-frequency product of HVT-NCFinFET are enhanced by ∼33.9%, 58.1%, and 50.3%, respectively, for drain underlap architecture (L_{dsu}) as compared to the baseline NC-FinFET. Further, we varied $N_{ch'}$, L_{dsu}, and $L_{g'}$ for trade-off performance compared to the baseline LVT-NCFinFET. Based on a comprehensive investigation, we found that the L_{dsu}-HVT technique is best suited for optimum performances. The Gummel symmetry test (GST) is also investigated as an additional linearity measure to the proposed HVT devices. Thus, the proposed HVT techniques analysis is worth exploring to obtain a proper design guideline for improved analog/RF and linearity performance of the NC-FinFET.

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