Multi Header Based Ultra Low Power MTCMOS Technique to Reduce NBTI Effect in Combinational Circuit.

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Abstract. With the advancement of technology , negative bias temperature instability (NBTI) emerges out as a major problem for VLSI circuits. Meanwhile, the leakage power increases dramatically as the supply/threshold voltage continues to scale down. These two issues present extreme unwavering quality issues for CMOS devices. Since both the NBTI and leakage are reliant on input test vector of the circuit however input vector control strategy isn't viable for bigger circuits. Thus in this paper two design is proposed (1) Single header Based Ultra low Power Diode Tri-mode Technique is designed for reducing leakage and delay of the circuit (2) Multi header Based Ultra low Power Diode Tri mode Technique with Body Bias on all sleep pMOS transistor to mitigate NBTI effect. Experimentations are done on 1 bit full adder circuit with the usage of tanner EDA at 90nm CMOS technology node and supply voltage 1V.The results reveal that by using first proposed technique leakage current is reduces by 74.93 % and 0.217% respectively as compare to Stacking with delay based MTCMOS method and ULP diode based MTCMOS method. First proposed design is also effective in terms of delay. Result shows that delay get reduced by 20.91% and 7.84% as compare to prevalent techniques. Second Proposed design at 50% Duty cycle is very much effective for NBTI effect mitigation. Experimental result shows that Second Proposed design with reduction in duty cycle(from 100% to 50%) the V_{th} shift on pMOS transistor reduces and with this decrement in V_{th} of pMOS transistor NBTI effect on the circuit will get reduced.

Keywords: Leakage reduction, Delay reduction, NBTI mitiga-tion, forward body biasing, reverse body biasing.

1 Introduction

As technology scales, the increment in leakage current and Negative Bias Temperature Instability (NBTI) are major problems to handle [1], [2]. The Leakage current contributes 50 % of the digital circuit operational power. The different types of powers of circuit like standby power, Active power and reliability of the circuit is affected by this. [3], [4]. When the circuit is in the OFF condition or say in standby mode then during this mode the standby power of circuit is get affected by the leakage current. So it is necessary to minimize leakage in standby mode for which a popular technique Power Gating is used with multi threshold (MTCMOS) transistors [5]. It is having a usage of high threshold sleep transistor which becomes inactive during standby mode as a result of which low Vth circuit gets isolated from supply voltage and ground in standby mode which as a result minimizes the leakage current. [5] [6]

The NBTI effects occurs in the p-type transistors when a logic “0” is used at the gate-to-source terminal, i.e. Vgs of pMOS transistor is negative bias (V_{gs} = V_{gs}) .This condition is called “stress state”, due to which the magnitude of threshold voltage(Vth) of the pMOS transistor increases over time. This increment of V_{th} the performance of the circuit. which shown in fig 1 . This is An primary thought in today's without limitations, is improve those execution of the circuit.

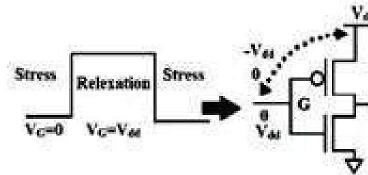

Fig. 1. Stress State on pMOS

After a long time this increment in V_{th} leads to further current degradation between the real Vdd and virtual Vdd line. It degrades the overall circuit performance with time. The Vth shift of pMOS can be controlled by (1) Body biasing and (2) Dividing stress time on parallel pMOS. [7]

In this paper different MTCMOS techniques are presented which uses concept of forward body biasing, reverse body biasing, diode connected transistor with parallel pMOS. [8] [9]. Different Standby leakage current, Delay improvement and Negative bias temperature instability aware power gat-ing technique are presented here. A comparative analysis of various power gating design along Vs and V_{bs} shows changes in reduction in delay and leakage

2. Related Techniques

Leakage current and life time of circuit is a most critical issue in VLSI industry. So, here we discuss related techniques in terms of leakage reduction and NBTI effect Mitigation.

2.1 STACKING TRANSISTOR WITH DELAY BASED MTCMOS CIRCUIT

In this technique, three transistor are use at the footer of low logic block in which N_1, N_2 are stacked and P_1 are connected in parallel with biasing, a current flowing through these sleep transistor which is controlled by C_1, The sub threshold leakage current equation (1) represents minimization in V_{ds} and the sub threshold leakage current when body to source voltage ($-V_{bs}$) increases

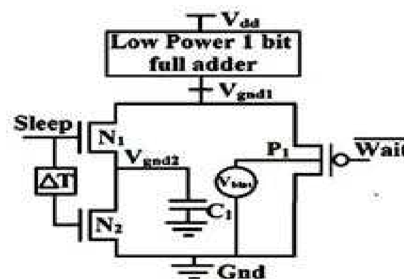

Fig. 3. Stacking transistor with delay based MTCMOS circuit

2.2 ULTRA LOW POWER DIODE BASED MTCMOS TECHNIQUE

The Ultra Low Power strategy is functioned as when diode is reverse bias both N_2 and P_2 works with negative V_{gs} voltage which prompts solid reduction of leakage current in equivalence with standard diode. At the point when V_{ds} voltage increased then diode reverse voltage increases

and current also increases.The current pass on the peak value and then strongly reduces with V_{gs} of transistor decorously more negative. P_1, P_2, N_1 and N_2 represents high threshold control gated ST's. In this method as comparison with diode connected method, the decrement in leakage current is more effective. [11] [13]

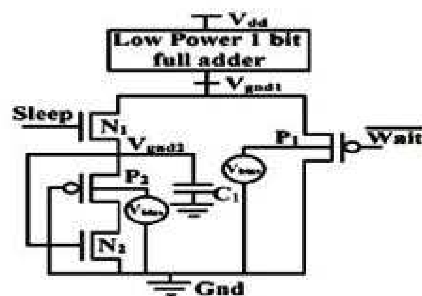

Fig. 4. Ultra low power diode based MTCMOS circuit

3. Proposed Design

3.1 Leakage aware Sıngle Header Based Ultra Low Power Dıode Trı Mode Technıque

In first proposed design , high vth transistor P_4 are connected head of the low logic block. N_1, N_2 sleep transistor are stacked with parallely connected P_1, P_2, and P_3 grip transistor . In active mode, P_1, P_2 and P_3 are forward body biased which reduced delay of circuit and in sleep mode, are reverse body biased grip transistor increases the V_{th} of the transistor as a result of which leakage is minimized in the sleep mode. In this design ,an additional Header pMOS transistor is added which is helpful to minimizes the circuit's wake up noise.

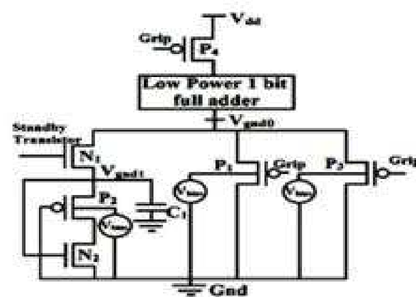

Fig. 5. Single header Based Ultra low Power Diode Tri mode Technique

3.2. NBTI Aware Multiheader Header Based ULP Dıode Technıque

In proposed design which is shown in Fig.6 N_1,N_2 sleep transistor are stacked and P_1,P_2,P_3 grip transistor are parallely connected.P_4 and P_5 are high threshold STs which are connected at the head of low logic block, the FBB is used to give the decrease in Vth of the transistor due to

which delay can be lowered in dynamic mode and RBB on sleep pMOS transistor in sleep mode to build the Vth of the transistor due to which leakage will be decreased in the sleep mode.

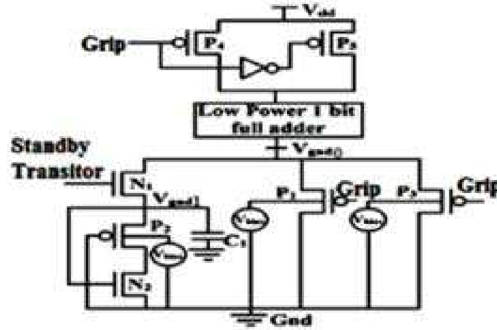

Fig. 6. NBTI Aware Two header Based Ultra low Power Diode Tri mode Technique

To relieve the NBTI issue in the circuit stress time is spilits into half on header transistors P_4 and P_5 of Fig.6. For this an inverter is utilized among transistors P_4 and P_5, by utilizing this inverter, when transistor P_5 is OFF the transistor P_4 will be ON and when transistor P_4 is OFF the transistor P_5 will be ON, along these lines the aggregate stress time splits over parallel header pMOS transistor. Along these lines stress time on single pMOS transistor decreases. The eq.(3) shows that stress time decreases the change in V_{th} because of NBTI likewise diminishes and it minimizes the lowering of current because of NBTI. that's why NBTI influenced circuit's aging time can be moved forward.

$$\text{Stress} : V_{gs} = -V_{dd} \rightarrow \Delta Vth \propto k_s\, e^{-Ea/KT} (t-t_{str})^{1/4.} \ldots\ldots\ldots\ldots\ldots(3)$$

The two factors Kv and kr whose significance relies on upon a some technical factors (such as channel strain and concentration of nitrogen), K represents Boltzmann steady, t represents nearby working temperature of the gadget and tstr represents time after that NBTI impact get presented. For numerical examination of NBTI impact in the circuit, condition (4), (5) and (6) are used to examine the shift in Vth along with variation in time .

$$\Delta V_{th} = K_v \ \beta^{\frac{1}{4}} (t)^{\frac{1}{4}} + \delta_v \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(4)$$

Where ΔV_{th} represents the variation in threshold voltage of pMOS (Threshold voltage shift), β is the duty cycle of active sleep pMOS transistor of power gating circuit and the duration after which NBTI aging effect comes into play is represented by t. The relationship between V_{th} and the V_{gs} is represented by equation(5) given below

$$K_v \propto \sqrt{C_{ox}(V_{gs} - V_{th})}\ \exp^{\frac{E_{ox}}{E_o}}\ \exp^{\frac{-Ea}{kT}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(5)$$

Where V_{th} is the threshold voltage of pMOS transistor and the oxide capacitance is represented by C_{ox} whose value is equal to 0.0135f, V_{gs} represents the gate to source voltage and K is the Boltzmann con-

stant and T is the temperature and Ea=0.13eV and δ_v =5mv and E0X and E0 =2mV are calculated by equation (6) .

$$E_{ox} = \frac{V_{gs} - V_{th}}{T_{ox}} \qquad (6)$$

4. METHODOLOGY

Next are the two activities on which stacking power gating configuration works :-

1. Reduction in subthreshold leakage current through stacked transistors.
2. Minimizing NBTI effect in active mode by reducing duty cycle at two header parallel pMOS.

4.1 Method to reduce leakage current in standby mode:

The leakage in OFF state can be effectively diminished to a degree with the assistance of stacking effect.In this technique all transistors are in off state for reducing the leakage current. By adding a header pMOS grip transistor with reverse body biasing,leakage current is reduced more effectively in sleep mode and delay is also reduces for batter performance of circuit

4.2. Method to reduce NBTI Effect:

In this method, A circuit shown below is proposed to reduce NBTI effect. Here we are including two (P_4 and P_5) header parallel pMOS grip transistor with forward body biasing for separating stress time (T_{stress}). This infers, for the first half time T_{stress} , P5 is OFF and P4 is ON, while for the other half-time frame, P5 is ON and P4 is OFF. Hence, both P4 and P5 are divide for half time so duty cycle will be half separated on these header transistor.Due to diving this time period of device performance will be improved and NBTI effect will get reduced more effectively.

5. SIMULATION RESULTS AND COMPARISON

The 90nm standard CMOS technology along with Tanner EDA was used for simulation of the circuit for 1-bit full adder circuit.(HighjV_{th}nMOS=320mV, lowV_{th}nMOS=72mV, HighjV_{th}pMOS=-273mV, lowV_{th}pMOS=-56mV, and V_{DD}=1V). Here the effectiveness of the single header based Ultra low Power Diode Tri mode Technique has been applied on 1 bit full adder circuits for the the delay and the leakage calculation.

5.1 . Leakage Analysis

In sleep mode, we apply a 0V to nMOS and 1V to pMOS then all sleep transistor will be in OFF condition. circuit is in sleep mode then we can analysis leakage effectively. All sleep transistor have large threshold voltage for reduction of leakage .

Table I represents the comparison between different techniques, by using pMOS transistor with reverse body bias on different techniques which reduces leakage current effectively.

Table I:leakage current analysis at different body biasing voltage

Power Gating Technique name	leakage current in pico amp with Body Bias voltage Vb				
	1.8v	1.2V	1 V	0.8V	0.4V
Stacking with delay	1087.1	1087.3	1087.5	1087.7	1088.1
ULP Diode based MTCMOS	272.8	272.99	273.18	273.37	273.76
Single header based ULP diodeTri mod	271.78	272.17	272.55	272.93	273.7

Table II. Leakage current result analysis for different power gating techniques with RBB voltage

Power Gating Technique name	leakage current in pico amp with Reverse Body Bias voltage Vb			Average Leakage Current
	1.4V	1.2V	1V	
Stacking with delay	1087.1	1087.3	1087.5	1087.3
ULP Diode based MTCMOS	272.8	272.99	273.18	272.99
Single header based ULP diodeTri mode	271.78	272.17	272.55	272.26

Table II shows the reduction of leakage for different power gating technique. Leakage depends upon the reverse body biasing variation so with the increment in biasing voltage leakage is reduced in single header based ULP diode tri-mode MTCMOS with reverse body biasing on sleep transistor method least leakage happens which is represented by the graph.

Table III. Leakage current analysis for 1 bit full adder for different power gated circuit with change in supply voltage

Power Gating Technique name	leakage current in pico amp with supply voltage V				
	1.4V	1.2V	1V	0.8V	0.4V
Stacking with delay	1157.1	1121.4	1087.5	105.5	920.63
ULP Diode based MTCMOS	143.27	197.13	273.18	366.01	504.18
Single header based ULP diode tri-mode	287.9	279.94	272.55	95.765	251.67

Table III demonstrates the relation of leakage current with voltage scaling .Extracted results are tabulated voltage downsize the leakage current is also decreases and with supply voltage increment the Leakage also expands in the circuit

5.2 . Performance Analysis in terms of delay.

Propagation delay shows the speed of any circuit, it is the combination of routing delay and gate delay in any circuit. In any circuit the duration needed by digital signal to travel from input to the output of the circuit is called propagation delay. Propagation delay may be different for any

circuit for different input combination. In any the delay is inversely related to the speed of the circuit so it is a essential factor to increase the speed of the system

Table IV. Delay result of different power gated circuit with change in bias voltage on pMOS sleep transistor

Power Gating Technique name	Delay in pico sec with Body Bias voltage Vb				
	1.4V	1.2V	1V	0.8V	0.4V
Stacking with delay	61.681	51.0487	42.781	35.475	24.328
ULP Diode based MTCMOS	40.32	38.503	35.543	31.46	22.897
Single header based ULP diode Tri-mode	40.704	38.85	35.845	31.801	23.081

Table IV result analyzes the delay of the distinctive power gated circuit with variation in V_{bs} on pMOS transistor in the circuit. From this table the outcome demonstrates is that speed of the circuit can be increased by using FBB in dynamic mode

Table V . Delay result of different power gated circuit with change in forward bias voltage on pMOS grip transistor

Power Gating Technique name	Delay in Pico sec with Forward Body Bias voltage		Average Delay(pico sec)
	0.8V	0.4V	
Stacking with delay	35.475	24.328	29.72367
ULP Diode based MTCMOS	31.546	22.897	27.17333
Single header based ULP diode Tri mode	31.801	23.081	27.391

Table V clearly shows the batter result in term of delay reduction using proposed single header based ULP diode based MTCMOS technique as compare to other technique

5.3. NBTI Effect Analysis

The V_{th} shift of the sleep pMOS header transistor along time increases. Result demonstrates that increase in stress time of grip pMOS transistor results increment in V_{th} shift. V_{th} shifting of sleep header transistor improves NBTI impacts in the circuit. Due to increment of NBTI effect reliability of circuit get reduced which is a major factor to improve.For improving this factor we divide Duty cycle(stress or on time) of grip pMOS header transistor.

Table VI Performance analysis of single Header based ULP diode Design and two header based NBTI aware ULP diode design (With 100% duty cycle)

Time(in sec)	New Vth in (V) after delta Vth shift	Delay in pico sec. with two transistor 100% duty cycle	Delay in pico sec. with single transistor 100% duty cycle
360000	0.273	19.783	19.641
361000	0.335918	19.799	19.453
362000	0.400367	45.101	43.101
363000	0.466353	59.556	50.292
364000	0.533885	233.1	232.1
365000	0.602971	252.02	252.02

Table VI demonstrates single header based ULP diode tri-mode design and Two header based ULP diode tri-mode method performance analysis with 100% duty cycle(during header sleep transistor).The results demonstrates the time increment which results in the increase in V_{th} shift of pMOS transistor and as a results of which threshold voltage of sleep pMOS transistor and Delay of the circuit likewise increases.

Table VII. Performance analysis of Header based ULP diode Design and NBTI aware Header Based ULP diode design (With 50% duty cycle)

Time in(Sec.)	New Vth in (V) after delta Vth shift	Delay in pico sec. with two transistor 50% duty cycle
360000	0.273	19.485
361000	0.326651	19.507
362000	0.381405	19.532
363000	0.437266	19.563
364000	0.49424	19.601
365000	0.55233	19.652

Table VII demonstrates the Two header based ULP diode tri-mode design performance analysis at half obligation(50%) on cycle of two header sleep transistor. The results shows the time increment as a result of which V_{th} shift of pMOS transistor also increases and with this increment in V_{th} of pMOS the circuit's delay also increases.

6. CONCLUSION

In this paper we have designed a circuit which improve leakage as well as delay and also propose a design which is very much effective to mitigate the NBTI effect. The results reveal that by using first proposed technique leakage current is reduces by 74.93 % and 0.217% respectively as compare to Stacking with delay based MTCMOS technique and ULP diode based MTCMOS technique. First proposed design is also effective in terms of delay.Result shows that delay get reduced by 20.91% and 7.84% respectively as compare to prevalent techniques. Second Proposed design at 50% Duty cycle is very much effective for NBTI effect mitigation. Experimental result shows that Second Proposed design with reduction in duty cycle(from 100% to 50%) the V_{th} shift on pMOS transistor reduces and with this decrement in V_{th} of pMOS transistor NBTI effect on the circuit will get reduced.

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