Temperature Insensitive Design For Power Gated Circuits

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***Abstract*—With rapid scaling in Deep Sub-micron (DSM) technologies, the difference between supply and threshold voltage is decreasing rapidly. This makes delay of the circuit highly sensitive to gate overdrive voltage with temperature fluctuations. In sub-100nm technologies, the delay of the circuit decreases with increase in temperature, known as Inverted Temperature Dependence(ITD) at nominal supply voltage. This effect was reverse in the older technologies. Scaling supply voltage further increases delay variation with temperature changes causing severe timing imbalance in the circuit. Further for a Power Gated circuit where a high threshold sleep transistor is inserted, timing is a critical issue. Temperature insensitive FBB with and without voltage scaling is proposed in the paper to achieve circuit tolerance to delay variations and hence temperature fluctuations.**

Keywords*—IT; Power Gating; FBB; Leakage; Temperature fluctuations.

I. Introduction

Scaling of CMOS devices into the sub-100nm domain has posed new challenges for the development of complex integrated circuits. Although, the benefits of scaling like high functional density,improved chip performance and lower IC cost [1] has surpassed the challenges. With millions of transistors integrated on a single chip the problem of heat dissipation and thermal management are of great concern. Scaling reduces the threshold voltage, supply voltage and oxide thickness. Due to reduction in supply voltage the dynamic power dissipation of the circuit has decreased which decreased the active power dissipation of the circuit. But due to threshold voltage scaling, the subthreshold leakage current has increased exponentially which is a major factor contributing to total leakage current. Also, due to thinner oxides other leakage mechanisms like GIDL, DIBL etc. are on rise too. Studies predict that leakage will consume upto 40% of total power consumed by a chip in deeply scaled technologies which is very large compared to older technologies. The leakage is expected to rise upto 32 times for every new technology node.

Due to exponential growth of leakage power combined with dynamic power dissipation, the power densities have also increased leading to more heat generation thereby increasing the operating temperature of IC's. Local hot spots formation can also take place at such high temperature. The combined effects of both high operating temperature and large temperature fluctuations poses a threat on circuit performance and reliability resulting in a large power dissipation and decreased circuit performance. Due to physical phenomenon like NBTI, Electomigration and Dielectric Breakdown the devices shows a slowdown thereby reducing circuit lifetime. The degradation severity is more pronounced at high temperatures.

The sub-100nm technologies shows a decreasing circuit delay curve with increase in temperature i.e. the circuit performance tends to increase with increase in temperature which is contrary to that found in earlier technologies. This phenomenon is recognized as ITD(Inverted Temperature Dependence). However the positive side to ITD is that circuit performs even better at higher temperatures. But the downside is the variation in delay of the circuit exposed to larger temperature fluctuations. The delay varies by as much as 20% in the scaled technologies thereby decreasing circuit robustness.

Figure 1 shows the decreasing ratio between supply voltage and threshold voltage at different technology nodes. The ratio is decreasing with each new technology node. Further, due to increasing use of multiple threshold transistors in digital circuit designing, the ITD effect has become more pronounced. For example, in this paper a popular leakage reduction technique known as "Power Gating" is used to minimize leakage of the circuit. Power Gating aims at cutting off the logic circuit from the supply rails or ground rails or both in standby mode, thereby disrupting the leakage current path in the circuit and hence minimizing leakage current. Power Gating makes use of high threshold and a larger sleep transistor which can be either PMOS or NMOS depending on the design criteria. The design in this paper focusses on NMOS sleep transistor insertion, the reasons for this is explained in Section II-B. The high V_{th} sleep transistor leads

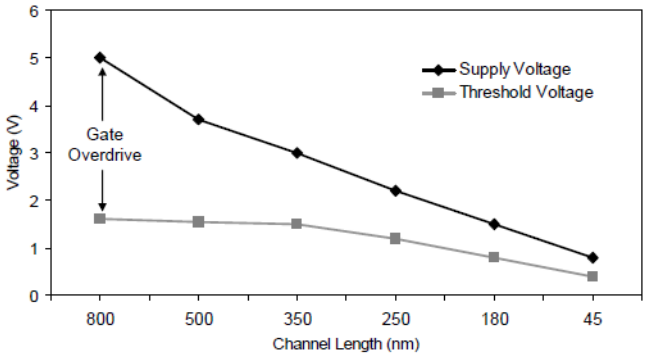

Fig. 1: Scaling of supply and threshold voltage at different technology nodes

to ITD phenomenon. From the equation,

$$\tau = \frac{1}{\mu(T)(V_{dd} - V_{th}(T))} \tag{1}$$

Delay depends on both Mobility and Gate Overdrive Voltage which are again a function of temperature. Thus, making delay as an indirect function of temperature. Use of high threshold transistors at scaled supply voltages makes the ratio $(V_{dd} - V_{th})$ vey small and hence highly sensitive to temperature. For sub-100nm technologies the gate overdrive variations generally dominates the mobility variations with temperature and hence decides the circuit delay dependence on temperature.

Thus, for a Power Gated design where circuit delay is a critical issue due to the ill effects of ST insertion, the presence of ITD in the circuit makes timing analysis a challenging task. The circuit performance can fail at a temperature other than maximum possible operating temperature due to unexpected circuit behaviour owing to ITD. The paper proposes two techniques to decrease the circuit delay variation with temperature fluctuations thereby increasing circuit tolerance.

The paper is organized as Section II describes the Background and Motivation for the paper. Section III discusses related work done on ITD phenomenon and the paper contribution to the same. Section IV discusses the simulation results and analysis on applying the proposed techniques on a Power Gated circuit. Section V concludes the paper.

II. Background And Motivation

This section briefly describes the effect of temperature on CMOS Physical Parameters for a 90nm technology node which will create a background in understanding ITD phenomenon.

A. Effect of Temperature On MOSFET Physical Parameters

The changes in circuit's temperature and thus delay effects circuit's speed, power and reliability directly. This section discusses the effect on MOS physical parameters like mobility,threshold voltage and drain current due to temperature variations which in turn effects circuit's performance.

$$T_c = T_0 + R_T I_d V_{ds} \tag{2}$$

where, T_c is the junction temperature, T_0 is the room temperature and R_T,I_d and V_{ds} indicates thermal resistance, drain current and voltage drop across MOSFET [2] respectively. Equation 2 shows how critical junction temperature increases when circuit enters into deep active mode thus creating changes in device mobility and threshold voltage with temperature and hence delay.

1) Effect on Mobility: The carrier mobility, μ (cm^2/Vs) describes the drift velocity of a particle in an applied electric field Under small to moderate electric fields [2].

$$\mu = \frac{v_d}{E} \tag{3}$$

where, v_d is the drift velocity, and E is the electric field. The temperature dependence of mobility is given as:

$$\mu(T) = \mu(T_0)(\frac{T_0}{T})^m \tag{4}$$

where T_0 is the reference temperature(300 K) and $\mu(T_0)$ is mobility at reference temperature, m is ideally 1 and $\mu(T)$ is mobility at desired temperature. From Equation 4 it is evident as temperature increases the mobility decreases which causes drain current to decrease and from Equation 1 the circuit delay also increases.

2) Effect On Threshold Voltage: The threshold voltage for a MOSFET is given as:

$$V_{th} = \phi_{gs} - \frac{\phi_{gs}}{C_{ox}} + 2\phi_f - \frac{Q_B}{C_{ox}} \tag{5}$$

and,

$$\phi_f = \frac{KT}{q} \ln \frac{n_i}{N_A} \tag{6}$$

where ϕ_f(fermi potential) and n_i(intrinsic concentration) are temperature dependent parameters which affects threshold voltage directly. The increase(decrease) in temperature decreases(increases) fermi potential of the device which affects threshold voltage in the same way. The temperature dependence of threshold voltage [3] can be represented as:

$$V_{th}(T) = V_{th}(T_0) - k(T - T_0) \tag{7}$$

where, T_0 is the reference temperature(300 K), $V_{th}(T_0)$ is the threshold voltage at reference temperature, k is the temperature coefficient which is around 0.8mV K^{-1} and $V_{th}(T)$ is threshold voltage at desired temperature. From Equation 7 it is evident that the threshold voltage decreases linearly with rise in temperature.

3) Effect On Drain Current: The drain current of MOSFET in saturation region is given as:

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2 \tag{8}$$

Out of all the parameters the temperature dependent parameters are only mobility and threshold voltage. Thus,

$$I_D \propto \mu(T)(V_{dd} - V_{th}(T))^\alpha \tag{9}$$

Sub-threshold leakage current is dependent on mobility and threshold voltage strongly. But these parameters effect the circuit in different ways. In particular lower mobility μ causes drain current to decrease; on the other hand, lower V_{th} causes the current to increase. The end result is that the drain current will show a direct or indirect temperature dependence, depending on the dominant parameter [4].

4) Effect on Circuit Delay:

$$\tau_P \propto \frac{C_{out}V_{dd}}{I_D} = \frac{C_{out}V_{dd}}{\mu(T)(V_{dd} - V_{th}(T))} \tag{10}$$

The above equation shows the circuit delay as a function of drain current which in turn is a function of mobility and threshold voltage and supply voltage.

- Thus, a decrease in μ degrades performance, while a decrease in V_{th} makes the device faster
- When using devices with larger V_{th}, the difference $(V_{dd} - V_{th}(T))$ becomes small, causing the delay to decrease as temperature increases. This phenomenon is referred to as **Inverted Temperature Dependence** (i.e., ITD)

B. MTCMOS Designing

Power Gating [5] is also referred to as MTCMOS Technique as it makes use of multi-threshold transistors in the circuit. In this, a transistor with high threshold voltage is inserted between power supplyreducing and existing design (PMOS or Header) or between ground rails and the logic circuit (NMOS or Footer) or both with externally controlled sleep signals. When the logic block functions normally during active mode i.e. when input and output transitions occur. The sleep signals are directed to turn on the corresponding PMOS or NMOS transistor on, this creates a direct conducting path between output and supply voltage and ground resulting in normal circuit operation. During sleep mode, the high threshold sleep transistor is turned off by controlling sleep signal. Thus, the direct current path is disrupted and the circuit is pushed into sleep mode. A new virtual supply voltage (PMOS) or virtual ground (NMOS) is created at source terminals of sleep transistors. Thus these transistors are known as sleep transistors as they forces the circuit into sleep or standby mode.

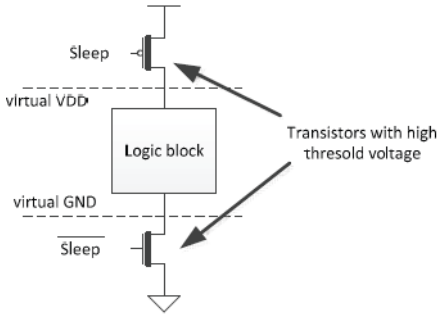

Fig. 2: Power Gating Concept

Figure 2 shows the sleep transistor insertion as a PMOS header or an NMOS footer. Either or both can be used for power gating , cutting the circuit from the power supply during standby mode.

Therefore, this technique requires fabrication of both high and normal threshold voltage transistors on a single chip. These high V_{th} sleep transistor acts as current gate for the designed circuit thus referred to as power gated circuit. Addition of a high V_{th} transistor effects the circuit delay in a negative way. Thus, sleep transistor designing is a critical step for circuit performance. There is a tradeoff between circuit speed, leakage power savings and noise immunity of MTCMOS circuit.

PMOS or Header insertion reduces circuit drive current and hence should be sized bigger to compensate for it. Also, PMOS suffers from NBTI (Negative Bias Temperature Instability) a reliability degradation mechanism which degrades PMOS transistor with time and is of major concern. Whereas NMOS or Footer insertion maintains driving current with smaller area but suffers from Ground Bounce Noise (GBN) problem. GBN creates spikes in the circuit when sleep transistor is turned on after sleep mode instantaneously and causes a large increase in drain current. This paper makes use of NMOS sleep transistor due to its inherent advantages.

III. Related Works And Paper Contributions

A. Related Works

ITD effect is known for quite some time for CMOS circuit and the same is addressed for non-power gated circuit in some recent works.

Calimera et.al [1] have proposed a temperature insensitive dual-V_{th} synthesis for nanometer CMOS under effect of ITD. The authors have proposed a threshold voltage assignment algorithm for dual V_{th} synthesis. This algorithm takes into account the temperature dependence of devices and yields low leakage circuit that are temperature insensitive.

The works of R.Kumar [6] proposes techniques for enhancing energy efficiency of circuit and also a technique to make the circuit temperature adaptive One is temperature adaptive dynamic supply voltage scaling which increases V_{dd} at high temperatures to maintain circuit consistency. While another technique which is Temperature adaptive body bias makes use of Reverse Body Bias at elevated temperatures to lower the leakage current [6] as well as increase the circuit threshold voltage V_{th} to such extent that the higher temperature circuit performance matches that of nominal V_{dd} at lowest operating temperatures.

The work in [7] suggests the use of forward body biasing to reduce circuit delay and to make circuit more robust against process and temperature variations which is an added advantage. FBB [8] is extensively used for increasing circuit performance but it increases power dissipation due to reduced threshold voltage whereas Reverse body biasing technique [8] reduces the power dissipation by increasing threshold voltage. There is also an upper limit to biasing voltages that can be used, like RBB is not justified below 45nm as it increases band to band tunneling current which compensates for decrease in subthreshold leakage current.

The above works focusses on non-power gated circuit and aims to achieve a low-leakage consistent circuit. The works in this paper aims in developing design techniques for making circuit delay insensitive to temperature fluctuations as well as improving circuit performance. Circuit delay minimization is the major design criteria as leakage is reduced by the use of power gating technique.

B. Paper Contributions

The paper uses power gating on a logic circuit to minimize leakage but the use of high threshold sleep transistor in the circuit leads to ITD effect as well as small speed degradation in the logic circuit due to its larger size and high V_{th}. Thus, the paper aims at improving circuit performance while keeping the circuit delay variation as minimum as possible.

1) Improved Circuit Performance: The proposed technique of using Forward Body Biasing at nominal V_{dd} at room temperature decreases the circuit delay due to reduced V_{th} therby decreasing circuit delay variations as well.

2) Reduced Delay Variations: The use of Forward Body Bias with voltage upscaling lessens the circuit delay variation to a minimum and also increases the circuit performance at upscaled supply voltage.

IV. Simulation Result And Analysis

A. Simulation Framework

The proposed techniques are applied on a Benchmark Circuit (C74283) 4-bit Carry Lookahead Adder Circuit which is widely used for performing arithematic addition operations in microprocessors. The circuit is designed in Static CMOS for 90-nm technology.The nominal supply voltage is 1V. Power Gating in form of NMOS sleep transistor is used for leakage minimization in the circuit. The threshold voltage of sleep transistor in 20% greater than the nominal threshold voltage used in circuit whereas its aspect ratio is upto 3 times larger than the largest transistor in the logic circuit. The proposed Forward Body Bias technique is applied on sleep transistor only, thus the entire circuit does not need to be changed for adjusting threshold voltage. This paper makes use of FBB technique which is less dependent on technology scaling.

B. Performance Analysis

The performance analysis of the circuit is done for typical, FF (Fast NMOS and Fast PMOS) and SS (Slow NMOS and Slow PMOS) process corners [9] to view the delay variation with circuit speed as well.

TABLE I: Sensitivity of parameters for 90nm node

90nm node	(Vgs – Vth) (V)		Mobility(cm^2/Vs)	
Temperature	**NMOS**	**PMOS**	**NMOS**	**PMOS**
25°C	0.260	-0.303	0.067	0.025
125°C	0.182	-0.381	0.043	0.016
Variation	30.76%	21.05%	24.62%	24%

Table I shows that the sensitivity of mobility is dominated by that of $(V_{gs} - V_{th})$. Thus, drain current increases with temperature causing delay to decrease.

- The Sleep signal is '1' for the NMOS sleep transistor. Hence it conducts and the circuit functions as normal.
- For circuit simulation all the inputs are simultaneously switched from 1 to 0. This creates a maximum discharge current and hence delay for the circuit.

The supply voltage is varied from 0.8V to 1.6V in steps of 200mV and the temperature is varied form 125^0C to 0^0C.

Table II shows the variation of delay at normal process corner. The delay variation at extreme temperatures is 6.35%.

TABLE II: Delay at typical process corner for temp. and V_{dd} variations

Temp.(°C)	Avg. Delay(ns)				
150	1.44	1.63	1.72	1.79	1.80
120	1.45	1.64	1.74	1.81	1.81
90	1.46	1.65	1.76	1.82	1.82
60	1.47	1.68	1.77	1.83	1.825
30	1.48	1.72	1.79	1.84	1.83
0	1.48	1.76	1.82	1.86	1.84
	0.8	**1**	**1.2**	**1.4**	**1.6**
	Supply voltage(V)				

TABLE III: Delay at FF process corner for temp. and V_{dd} variations

Temp.(°C)	Avg.Delay(ns)				
150	0.59	1.60	1.72	1.78	1.89
120	0.61	1.65	1.73	1.79	1.90
90	0.62	1.65	1.75	1.80	2.05
60	0.64	1.67	1.76	1.82	2.06
30	0.66	1.674	1.77	1.84	2.07
0	0.71	1.68	1.78	1.86	2.08
	0.8	**1**	**1.2**	**1.4**	**1.6**
	Supply voltage(V)				

Table III shows the delay variation at FF process corner. The delay variation at temperature boundaries is 3.61%.

TABLE IV: Delay at SS process corner for temp. and V_{dd} variations

Temp.(°C)	Avg. Delay(ns)				
150	1.47	1.62	1.73	1.79	1.80
120	1.46	1.64	1.75	1.796	1.81
90	1.45	1.66	1.76	1.798	1.83
60	1.43	1.69	1.78	1.80	1.84
30	1.423	1.71	1.80	1.81	1.86
0	1.41	1.73	1.82	1.82	1.88
	0.8	**1**	**1.2**	**1.4**	**1.6**
	Supply Voltage(V)				

Table IV shows the variation of delay at SS process corner. The delay variation is found to be 7.38%.

Figure 3 shows the delay variation with temperature at typical process corner. It is evident as supply voltage increases the delay variation decreases but at the cost of increased circuit delay and the opposite happens when supply voltage is downscaled. The delay variation at supply voltage of 0.8V, 1V and 1.2V are 20%, 5.26% and 1.11% respectively.

From the analysis FF corner and SS Corner shows the

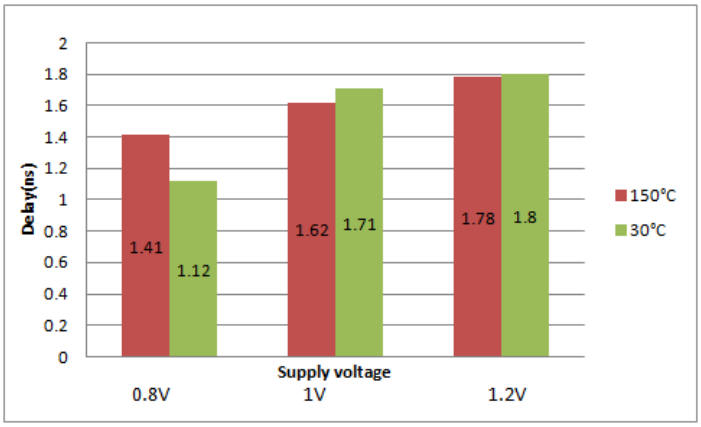

Fig. 3: Delay variation at different supply voltages

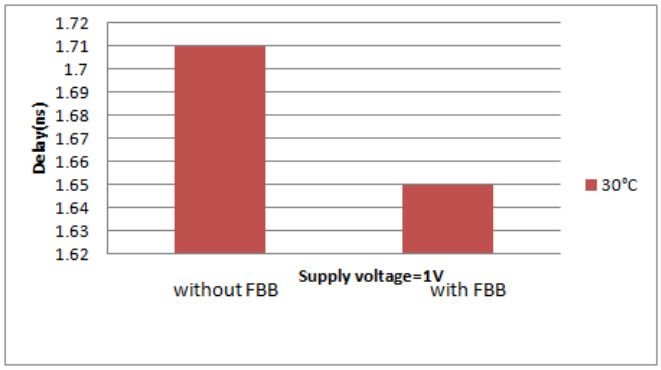

Fig. 4: Delay comparison of 4-bit CLA circuit with and witout FBB at nominal V_{dd}

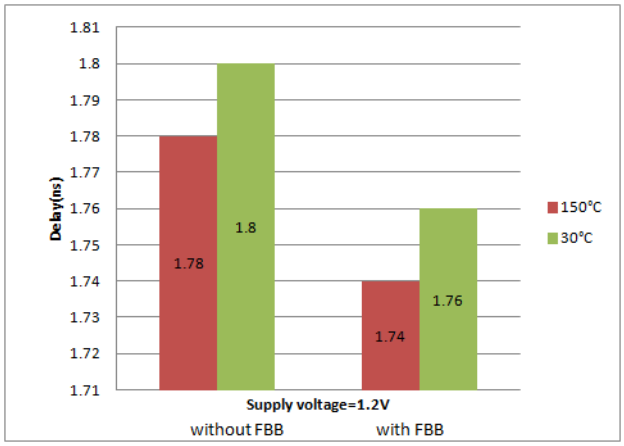

Fig. 5: Delay comparison of 4-bit CLA circuit with and witout FBB at scaled V_{dd} = 1.2V

small(high) variation due to low V_{th}(high V_{th}) transistors used thus decreasing(increasing) the delay sensitivity to gate overdrive voltage.

C. Simulation Results For Proposed Techniques

There are two proposed techniques in this paper. One is use of Forward Body Biasing at nominal supply voltage for reducing delay variation and the other is use of Forward Body Biasing at scaled supply voltages for improving circuit performance and also delay variation with temperature. The circuit can be operated at low supply voltages with Forward Body Bias for smaller Power Delay Products (PDP). It is defined as

TABLE V: Power Delay Product Variations with supply Voltages And Temperature

Temp.	Delay (ns)	Power (µW)	PDP (1e-15 Joules)	Delay (ns)	Power (µW)	PDP (1e-15 Joules)	Delay (ns)	Power (µW)	PDP (1e15 Joules)
125°C	1.128	26.33	29.70	1.62	43.92	71.15	1.78	85.72	152.58
25°C	1.42	23.04	25.87	1.71	40.82	69.80	1.80	69.54	125.17
Vdd	**0.8V**			**1V**			**1.2V**		

product of delay of the circuit with power dissipation of the circuit. It should be minimum as possible. Table V compares the variation of PDP's at different supply voltages. There is a reduction in PDP of upto **62.5%** compared to that of nominal V_{dd}. But this technique suffers from a major problem of heightened delay sensitivity to temperature for which the circuit should be extremely tolerant.

The supply voltages can be increased to increase temperature insensitivity from Table 3 but the circuit delay increases by upto 5% which is significant for long-term operation. The use of forward body biasing at room temperature can be done to reduce the circuit delay at room temperature while maintaining the temperature insensitivity.

Figure 4 shows the delay comparison at room temperature at a FBB of 0.5V. The delay variation reduces to **1.81%** compared to 5% in table 3. Figure 5 shows the delay variation at room and increased circuit temperature for elevated supply voltage of 1.2V. The delay decreases by **2.24%** at room temperature and the delay variation remains consistent at **1.11%**.

V. Conclusion

The delay sensitivity to gate overdrive voltages induces delay variation with temperature fluctuations in sub-100nm technologies. This problem is more pronounced in power gated circuit due to use of high threshold sleep transistors which contibutes to ITD effect. By using Forward Body Bias at room temperature and nominal supply voltage successfully reduced the delay variations to 1.81%. While using Forward Body Bias with voltage scaling keeps the circuit delay variation consistent at 1.11% but increases the circuit performance by 2.3%. Further the use of FBB at lower supply voltages decreased the PDP of the circuit by 62.5% which came at the cost of increased delay variation. Thus,when circuit performance is a major design goal as in power gated circuits the use of FBB with voltage scaling is an optimum solution. Although there is little increase in leakage current of the circuit compared to one without body biasing due to decreased threshold voltage of sleep transistor. Thus the threshold voltage of sleep transistor

is made higher than rest of the transistors to compensate for the increased leakage.

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