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An Efficient Design Approach for Low Leakage & High Performance MTCMOS Circuit; with NBTI Aware Analysis

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***Abstract*— As the technology scales down the leakage current in the circuit increases due to reduction in threshold voltage and Negative Bias Temperature Instability (NBTI) producing aging effect in the circuit. Leakage current and NBTI strongly depends on Input Vector Control Technique (IVC) , but IVC is not effective for larger circuits. Therefore in this paper two new designs (1)Ultra low power diode based technique with body biasing on both sleep pMOS transistors and (2)Ultra low power diode based technique with Parallel sleep pMOS and body biasing on all sleep pMOS to reduce leakage and delay of the circuit and a third design (3)Ultra low power diode based technique with delay on parallel sleep pMOS and Body Biasing on all sleep pMOS for reducing NBTI degradation of the circuit are proposed. Experimentations are done on 1 bit full adder circuit at 90nm technology node and supply voltage 1V.The results reveal that leakage current reduces by 81.73% using Ultra low power diode based technique with body biasing on both sleep pMOS transistors and 81.76% by using Ultra low power diode base technique with Parallel pMOS and body biasing on all sleep pMOS transistors and delay reduces by 15.31% and 15.41% respectively of the circuit.**

***Index Terms*— Leakage reduction, Delay reduction, NBTI mitigation, forward body biasing, Reverse body biasing.**

I. INTRODUCTION

As technology scales, the increment in leakage current and Negative Bias Temperature Instability (NBTI) are major problems to handle [2][10]. The Leakage current contributes 50 % of the digital circuit operational power. It affects the different power types of the circuit like standby Power, Active Power and Reliability of the circuit[1][2][3]. When the circuit is in the off condition or say in standby mode then leakage current in this mode affects the standby power of the circuit. So it is important to reduce leakage in standby mode for which a popular technique Power Gating is used with multi threshold (MTCMOS) transistors [12]. It uses high threshold sleep transistor which turns off in standby mode so that low threshold voltage circuit is disconnected with supply voltage and ground in standby mode which reduces the leakage current as shown in Fig.1.[7]

The NBTI effects occurs in the p-type transistors when a logic "0" is applied at the gate-to-source terminal, i.e. gate to source voltage of pMOS transistor is negative bias (V_{gs}= -V_{dd}) .This condition is called "stress state", due to which the magnitude of threshold voltage(V_{th}) of the pMOS transistor increases over time.

After a long time this increment in V_{th} leads to further current degradation between the real $V_{dd}$and virtual V_{dd} line. It degrades the overall circuit performance with time. The V_{th}shift of pMOS can be controlled by (1) Body biasing and (2) Dividing stress time on parallel pMOS.[10]
Leakage can be controlled by using Reverse body biasing in standby mode on pMOS, in which body to source voltage $V_{bs}$is greater than supply voltage V_{dd}. It increases the $V_{th}$of the transistor, reducing the leakage current. Delay can be controlled by using Forward Body biasing on pMOS in active mode of the circuit, in which body to source voltage V_{bs} is less than V_{dd},so the $V_{th}$of the transistor reduces thereby reducing delay.
In this paper different MTCMOS techniques are presented which uses concept of forward body biasing, reverse body biasing, Ultra low power diode with parallel pMOSand Adaptive body biasing[10][11]. Different Standby leakage current, Delay improvement and Negative bias temperature instability aware power gating technique are presented here. A comparison analysis of different power gating design with supply voltage and body bias voltage represents the modification in leakage reduction and delay reduction.

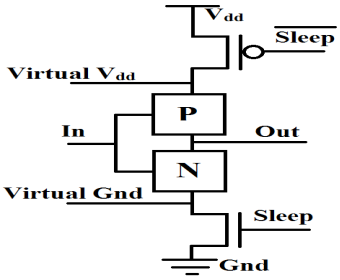

Fig.1 Power gated circuit

II. Standby Leakage Current Reduction Technique

Previous Work

A. Stacking sleep transistor with delay

In this technique N_1, N_2 and P_1 are high threshold sleep transistors and body biasing is done on P_1 transistor. C_1 is used to control the drain current flowing through the sleep transistor. The sub threshold leakage current equation (1) shows that when negative bias voltage V_{bs} increases and drain to source voltage V_{ds} decreases, the sub threshold leakage current reduces.

$$I_{SUB} = Ae^{\frac{q}{nkT}(V_{gs}-V_{th0}+\gamma V_{bs}+nV_{ds})}\left(1-e^{\frac{-qV_{ds}}{kT}}\right) \quad (1)$$

$$A = u_n C_{ox}\frac{W}{L}\left(\frac{KT}{q}\right)^2 e^{1.8} \quad (2)$$

When circuit of Fig.2 is in standby mode, the transistors N_1, N_2 and P_1 are turned off. The intermediate voltage V_{gnd2} is charged to some positive potential due to small drain current of transistor N_1. So due to this positive voltage at intermediate node, the potential of drain to source (V_{ds1}) of N_1 reduces. So drain induced barrier lowering also reduces and negative body to source voltage (V_{bs1}) of transistor N_1 further increases the body effect. In this way leakage is reduced more effectively. [5][8][14][11]

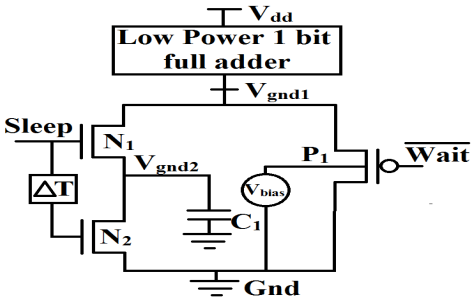

Fig.2 Stacking transistor with delay based MTCMOS circuit

III. PROPOSED DESIGN

A. Ultra low power diode based technique with body biasing on both sleep pMOS transistors

The ultra low power diode based design with body biasing is shown in Fig.3. In the proposed design, N_1, N_2, P_1 and P_2 are the high threshold power gated sleep transistors. P_2 and N_2 make an Ultra low power diode[9][11][13] and stacking of transistors is done to reduce the leakage, as discussed in section 2.1[5]. The weak inversion current equation of transistor P_2 and N_2 are given in equation (3) and (4).

$$I_{d,N_2} = I_{sno} e^{\frac{V_{gs,N_2}}{nV_T}} e^{\frac{\eta V_{ds,N_2}}{nV_T}} \left(1 - e^{\frac{-V_{ds,N_2}}{V_T}}\right) \quad (3)$$

$$I_{d,P_2} = I_{spo} e^{-\frac{V_{gs,P_2}}{nV_T}} e^{\frac{\eta V_{ds,P_2}}{nV_T}} \left(1 - e^{\frac{-V_{ds,P_2}}{V_T}}\right) \quad (4)$$

Where $V_{gs}$and V_{ds} are gate-to-source and drain-to-source voltage respectively, n is body coefficient, V_T = kT/q is the thermal voltage and η is drain induced barrier lowering (DIBL) coefficient. I_{sno} and I_{spo} are reference currents that correspond to the extrapolation of weak inversion drain current for V_{gs}=0 and V_{ds} in saturation (but low enough to neglect DIBL). In standby mode ultra low power diode is in reverse bias condition, so sleep transistor P_2 and N_2 are operating with negative V_{gs} voltage. There is strong leakage reduction due to this ultra low power diode. The leakage current is reduced more effectively than diode connected design.

To further reduce the leakage current to a considerable amount, we use reverse body bias on both pMOS power gated sleep transistors P_1 and P_2. The leakage current is directly related to threshold voltage of the transistor, similar to the current equation in (1). So by using reverse body biasing on all sleep pMOS transistors, in which body-to-source voltage $V_{bs}$of sleep pMOS transistor is less then supply voltage V_{dd}; V_{th} of the transistors increases, reducing the leakage more effectively.

Similarly when circuit goes to active mode then we use forward body biasing on all sleep pMOS transistors, in which body-to-source voltage $V_{bs}$is greater than supply voltage V_{dd}. Delay of CMOS circuit is shown in equation (5). [4]

$$Delay = \frac{C_{load}(V_{dd}/2)}{kW(V_{dd}-V_{th})} \quad (5)$$

whereC_{load} is load capacitance, $V_{dd}$is supply voltage and V_{th} is threshold voltage of transistor. When forward body biasing is applied on sleep pMOS transistors in active mode, the $V_{th}$of transistor reduces, decreasing the overall delay of the circuit.

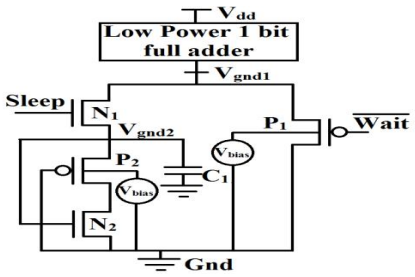

Fig .3 Ultra low power diode based MTCMOS technique with body biasing on sleep transistor P_1 and P_2

B. Ultra low power diode based technique with Parallel sleep pMOS and body biasing on all sleep pMOS transistors

The next proposed method uses Ultra low power diode based parallel sleep pMOS and body biasing on all sleep pMOS transistors design as shown in Fig.4. Here N_1, N_2, P_1, P_2 and P_3 are the high threshold sleep transistors. C_1 is the capacitor use to control the drain current of the N_2 transistor. The ultra low power diode works in a similar way as discussed in section 3.1 and leakage also reduces by stacking of transistors[5][9] [11]. The proposed design uses one more parallel sleep transistor P_3.The width of sleep transistors P_1 and P_3 (Fig.4) is half of the width of transistor P_1 of Fig.3. The leakage current is directly proportional to the W (width) of transistor and inversely to L (Length) of transistor, as shown in equation (1) and (2). So when W is becomes W/2 and L remains same, the leakage will be reduced more effectively than the W of a single pMOS transistor P_1 of Fig.3. The leakage can be further reduced by using reverse body biasing on sleep

pMOS P_1, P_2 and P_3 transistors, as it increases the threshold voltage of the transistors and reduces leakage current more effectively.

By using forward body biasing in active mode, as shown in Fig.4, the $V_{th}$of the pMOS sleep transistor reduces. As in equation (5), if $V_{th}$of transistor reduces, the delay will also reduce [4]. So if forward body biasing increases in active mode i.e. satisfying $V_{bs}>V_{dd}$, then the delay will reduce more effectively. [10]

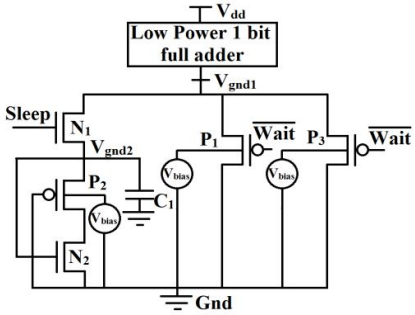

Fig.4 Ultra low power diode based MTCMOS technique with Parallel pMOS and body biasing on P_1, P_2 and P_3

C. NBTI Aware Ultra low power diode based technique with Parallel sleep pMOS transistors and body biasing on all sleep pMOS transistors

A NBTI aware design is proposed as in Fig.5. In this design N_1, N_2, P_1, P_2 and P_3 are high threshold sleep transistors. The working of ultra low power diode (as discussed in section 3.1), and stacking of transistors (as discussed in section 2.1), shows reduction in leakage [5][9][11]. The forward body biasing on all sleep pMOS transistors as in given Fig.5, reduces the V_{th} of the transistor, so that delay can be reduced in active mode and can provide reverse body biasing on all sleep pMOS transistors of design in sleep mode, to increase the $V_{th}$of the transistor. Due to this leakage will be reduced in the sleep mode, more effectively, as discussed in section 3.2.

NBTI aging effects occur only during stress; therefore, the larger the zero probability of the sleep signal, the larger the aging of the sleep-transistor characteristics. However, the static zero probability of the sleep signal is not a free design variable by itself; it depends on the actual workload and the resulting idle periods of the circuit. Nevertheless, it is possible to distributethe NBTI-induced stress over multiple sleep transistors [10]. The stress equation of pMOS transistor is given as

$$when\ V_{gs} = -V_{dd} \rightarrow \Delta V_{th} \propto k_s e^{\frac{-E_a}{kT}} (t - t_{str})^{\frac{1}{4}} \qquad (6)$$

where k_v and $k_r$are two parameters whose magnitude depends on a few technological parameters (like channel strain and nitrogen concentration), kis the Boltzmann constant, Tis the local operating temperature of the device, E_a is a technology independent parameter that guarantees the convergence of the model, and t_{str} isthe time at which the stress phases begins. NBTI effect is introduced in the system only when $t>t_{str}$. By equation (6), if t increases, then V_{th}shift also increases; because V_{th} shift is directly proportional to ¼ th power of time t.

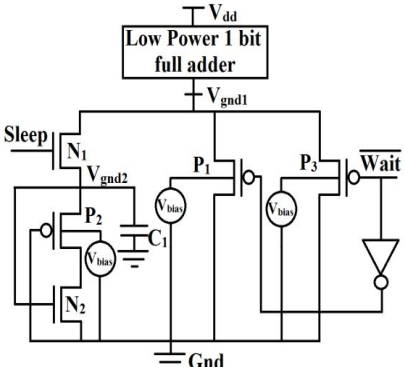

Fig .5 Ultra low power diode based MTCMOS technique with Parallel pMOS and body biasing on sleep transistor P_1, P_2 and P_3 with delay

To mitigate the NBTI problem in the circuit, we divide the stress time on transistor P_1 and P_3 of ultra low power diode based parallel pMOS design. For this a delay is used between transistor P_1 and P_3.By using this delay, when transistor P_3 is on, the Transistor P_1 will be off and when transistor P_1 is on, the transistor P_3 will be off. In this way the total stress time on sleep pMOS P_1 and P_3 (in Fig.4) becomes half in Fig.5. If stress time on single sleep pMOS P_1 or P_3 reduces, then by equation (6), the V_{th}shift also reduces. Due to this, NBTI degradation also reduces.

Body biasing represents an attractive solution for NBTI-aware design. By using Forward body biasing (FBB) in active mode, the V_{th}shift can be reduced, so in turn NBTI degradation can be reduced more effectively.

IV. Simulation of Previous & Proposed Power Gated Approaches on One Bit Full Adder Circuit and Result Analysis

A. Leakage Analysis

Standby leakage current is measured when circuit is in standby mode. In standby mode sleep transistor of power gated circuit are off by giving input 0V to nMOS and 1V to pMOS. The threshold voltage of power gated transistors is kept high to reduce the leakage current. The standby leakage current is different for different input combination.

The leakage current analysis of one bit full adder is shown in Fig.6 [6]. It shows that leakage current is different for different input combinations and is minimum for the input combination, A=0, B=0 and C=0. So while in standby mode, the input vector combination A=0, B=0 and C=0 is taken for minimum leakage.

The simulation result of table I represents the comparison between different technique when applying the reverse body biasing (RBB) on the pMOS power gated transistor in different power gating techniques (including the proposed technique). The leakage current reduces more effectively when RBB is used and when FBB is used, the leakage current increases as shown in the Fig.7.

Table 2 shows the comparison between the different techniques with reverse body biasing. It shows that the Ultra low power diode with parallel pMOS technique is best for the leakage reduction, in comparison to other technique, and by providing the delay on pMOS, stress can be reduced on pMOS sleep transistor. So, NBTI aging can be minimized, but it also results in the increased average leakage, as compared to other techniques.

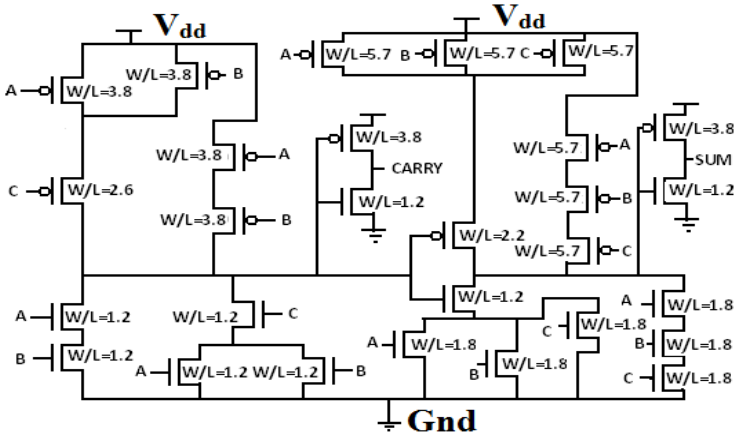

Fig.6 The circuit diagram of 1 bit full adder

TABLE I. LEAKAGE CURRENT RESULTS FOR DIFFERENT POWER GATING TECHNIQUE WITH CHANGE IN BODY BIAS VOLTAGE

Technique name	Leakage current in Pico-amp. with Body Bias voltage V_b						Average leakage(Pico- amp.)
	1.4V	1.2V	1V	0.8V	0.6V	0.4V	
Stacking with delay	1087.1	1087.3	1087.5	1087.7	1087.9	1088.1	1087.6
ULP diode with Body biasing on both pMOS	132.63	191.11	273.18	375.23	474.74	543.32	331.7016667
ULP diode with Parallel PMOS MTCMOS	131.71	190.36	272.61	374.83	474.51	543.28	331.2166667
ULP diode with Parallel PMOS with delay MTCMOS	1815.8	2727.5	4119.1	6249.9	9523.9	1458.6	6503

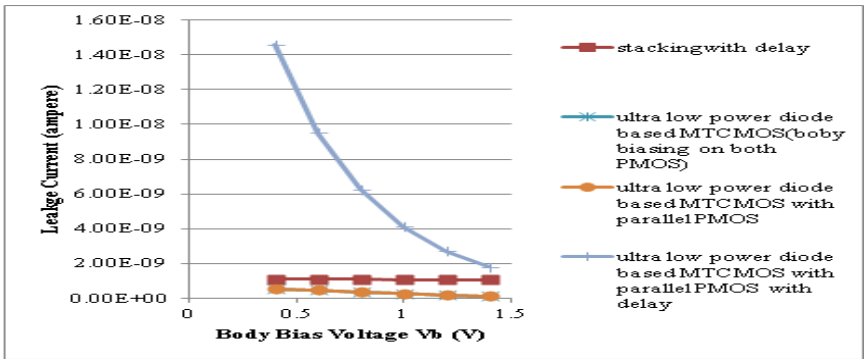

Fig.7 Leakage current variation with different body bias voltage

TABLE II. LEAKAGE CURRENT RESULT ANALYSIS FOR DIFFERENT POWER GATING TECHNIQUE WITH REVERSE BODY BIAS VOLTAGE

Technique name	Leakage current in Pico-amp. with Body Bias voltage V_b			Average leakage(pico amp.)
	1.4V	1.2V	1V	
Stacking with delay	1087.1	1087.3	1087.5	1087.3
ULP diode with Body biasing on both pMOS	132.63	191.11	273.18	198.9733333
ULP diode with Parallel PMOS MTCMOS	131.71	190.36	272.61	198.2266667
ULP diode with Parallel PMOS with delay MTCMOS	1815.8	2727.5	4119.1	2887.466667

TABLE III. DELAY RESULT OF DIFFERENT POWER GATED CIRCUIT WITH CHANGE IN BIAS VOLTAGE ON PMOS SLEEP TRANSISTOR

Technique name	Delay in Pico-sec. with Body Bias voltage V_b						Average Delay(Pico-sec.)
	1.4V	1.2V	1V	0.8V	0.6V	0.4V	
Stacking with delay	61.7	51.5	42.8	35.5	29.4	24.3	40.86666667
ULP diode with Body biasing on both pMOS	53.2	43.3	35.5	29.4	24.7	21.4	34.58333333
ULP diode with Parallel PMOS MTCMOS	53.1	43.3	35.5	29.3	24.7	21.4	34.55
ULP diode with Parallel PMOS with delay MTCMOS	57.1	46.3	37.9	31.2	26.5	23.4	37.06666667

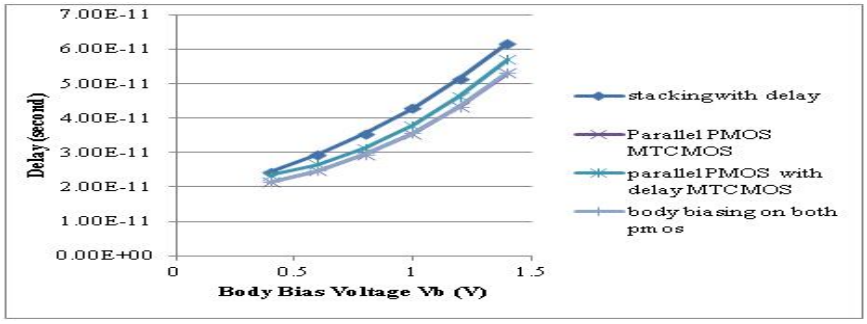

Fig.8 Delay comparison graph of different design with Body biasing voltage

B. Performance Analysis

Propagation delay shows the speed of any circuit. It is the combination of routing delay and gate delay in any circuit. In any circuit propagation delay is the time required for a digital signal to transfer from the input(s) to the output of the circuit. Propagation delay may vary with varying input combination, for any given circuit. Delay of any circuit is inversely proportional to the speed of the circuit, so it is an important parameter to increase the speed of the system.

Table 3 compares the delay of the different power gated circuit, which changes with change in body bias voltage on pMOS sleep transistor in the circuit. The results of this table shows that by using forward body biasing in active mode, the speed of the circuit can be improved and by using reverse body biasing the circuit speed will be reduced. The delay results are shown in Fig.8.

V. Conclusion

Leakage Power, Speed and Reliability of the circuit are the major goals with technology scaling. In this paper we have proposed two leakage and delay improvement techniques and a modification in this technique to mitigate the NBTI degradation. Both, Ultra low power diode with body bias on both pMOS and Ultra low power diode with parallel pMOS and body biasing on these pMOS transistor, are capable to achieve better results in leakage and delay analysis as compared to other power gating techniques. A small area overhead occurs, but it gives better results in leakage current and delay minimization. The ultra low power diode with body biasing on both pMOS provides 81.70% better results than Stacking sleep transistor with delay and delay reduction improvement is 15.31% by using forward body biasing in active mode. The simulation results show that the leakage can be improved by 81.76% using ultra low power diode with parallel pMOS sleep transistors with body biasing in comparison to Stacking sleep transistor with delay technique and delay improves by 15.41%.

VI. Future Work

The proposed design approach , "NBTI Aware Ultra low power diode based technique with Parallel sleep pMOS transistor and body biasing on all sleep pMOStransistors" for NBTI aware MTCMOS circuit shows a improvement in delay and leakage current of the circuit. The design can be further modified for leakage and delay improvements along with NBTI mitigation.

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