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A New Design Technique to Reduce the Ground Bounce Noise and Leakage in Four bit Binary Adder Circuit

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Abstract- **The performance degradation with technology scaling is one of the major issues in today's life. Leakage power dissipation in the IC increases exponentially with technology continuously scaling down. Multi threshold CMOS Power Gating is a very well known way to reduce leakage current, but when circuit transition goes from sleep to active mode, due to abrupt transitions introduces Ground Bounce Noise in the circuit, it disturbs the normal working of any circuit and tends to wrong output and also reduces the reliability of circuit. In this paper two effective Power Gating techniques "Ultra low power (ULP) diode based technique with parallel sleep pMOS transistors" and "Single header based Ultra Low Power diode with parallel sleep pMOS transistors" are proposed. These are dealing with Ground Bounce Noise and Leakage problem in the circuit. For that an additional wait mode and extra header transistor is added in the circuit to reduce the ground bounce noise. A comparison analysis between existing and proposed power gating techniques has been done on 90nm technology node, which shows that the proposed techniques "Ultra low power diode based technique with parallel sleep pMOS transistors" and "Single header based ultra Low Power diode with parallel sleep pMOs transistors" reduces leakage by 70.40 and 70.70% respectively and ground bounce noise by 10.38, 14.02% respectively in comparison to Diode Based trimode power gating technique..**

Keywords-**Ground Bounce Noise, Leakage current, Ultra Low Power Diode, Body biasing**

I. Introduction

In advance CMOS technology with technology scaling the supply voltage and the threshold voltage also continuously scaling down, due to which leakage power dissipation increases in the circuit, it is one of the biggest challenges related to low power designs in today's life. Multi threshold CMOS Power Gating is an efficient technique to suppress the Leakage current, and to reduce the Leakage Power in the circuit in standby mode [1][2][16]. In this power gating technique, a High Threshold (High-V_{th}) transistor is added either between Supply Rail and Logic block (Header) or Logic block and Ground Rail (Footer), or a combination of both is used [4]. MTCMOS Power Gating is a technique in which certain part of the chip turned off, when chip is idle. At the same time, during low V_{th} circuit mode transition from sleep mode to active mode, power gated circuit suffers from ground Bounce Current due to sudden discharge path from virtual V_{dd} to Ground line, as shown in Fig.1, which results from parasitic inductance of circuit [3]. High Threshold voltage for sleep transistor is chosen due to fact that it restricts the leakage current and Logic block consists of low voltage transistors to increase the performance of the circuit.[7][9]

In Fig.1 drain of the high threshold nMOS sleep transistor is at voltage H" V_{dd}, when circuit is in standby mode the both sleep transistor are turned off so low V_{th} block is disconnected from supply and ground and leakage reduces, but when these transistors switches from sleep mode to active mode, a surge current flows due to discharge of the drain terminal of nMOS sleep transistor, known as Ground Bounce Noise. Due to Current surge produced during switching between sleep to active mode MTCMOS Power Gating technique needs to special attention to improve the reliability of the circuit.

Various MTCMOS techniques like tri-transistor controlled MTCMOS, Dual switch MTCMOS, diode based trimode has been proposed in past for reducing the leakage current in standby mode and ground bounce noise (GBN) in sleep to active mode transition of the circuit [8][13][15]. In various power gating design uses the concept of extra wait state to reduce the ground bounce noise [14]. In this paper different multi threshold CMOS technique has been presented which uses the concept of forward body biasing (FBB), reverse body biasing (RBB) and ultra low power diode. Ground Bounce noise during mode transition of sleep to active and leakage phenomena in standby mode is investigated in this paper.

Organization of the paper is as follows: Diode based trimode power gating is discussed in section II, different proposed leakage reduction and ground bounce reduction techniques are discussed in section III, comparison analysis of different power gating techniques for leakage and ground bounce noise with change in body bias voltage, supply voltage, temperature and wait transistor resizing is discussed in section IV, further reduction of ground bounce noise in proposed design with body bias voltage and transistor resizing is discussed in section V, which is followed by Conclusion in Section VI.

II. Diode Based Trimode Technique

Diode Based Trimode Power gating technique shown in (Fig.2). In this technique N_1, N_2 and P_1 are high threshold sleep nMOS and pMOS transistors. To make a CMOS diode the gate of N_2 transistor is connected to drain of N_1 transistor and transistor N_1 and N_2 are connected in series to make transistor stacking to reduce the leakage current [5][11].The

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capacitor C_1 is connected as shown in Fig.2 to control the drain current of N_1 transistor and to control the intermediate node voltage V_{gnd2}. An additional wait mode is being introduced between sleep to active mode transition of circuit by adding an extra pMOS transistor P_1 in parallel [8]. Due to this there are total three modes of operation sleep, wait and active.

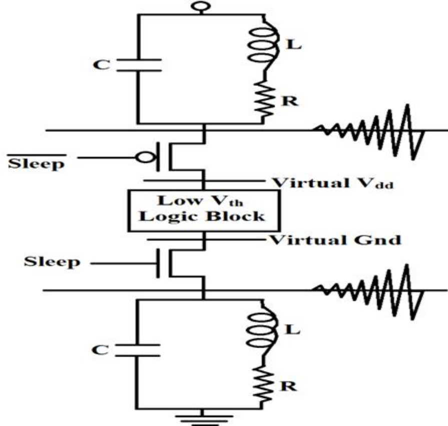

Fig.1 Power gating circuit

The sub threshold Leakage current expression is given by equation (1). [5]

$$I_{SUB} = Ae^{\frac{q}{nkT}(V_{gs}-V_{tho}+\gamma V_{bs}+nV_{ds})}\left(1-e^{\frac{-qV_{ds}}{kT}}\right) \quad (1)$$

$$A = u_n C_{ox}\frac{W}{L}\left(\frac{KT}{q}\right)^2 e^{1.8} \quad (2)$$

V_{gs},V_{bs} and V_{ds} are the gate to source, bulk to source and drain to source voltages respectively. V_{th0} is the zero bias threshold voltage, C_{ox} is the gate oxide capacitance and μ_n is mobility. η is the drain induced barrier lowering coefficient (DIBL) and γ is the body effect coefficient. Equation (1) and (2) shows leakage current reduces exponentially when drain to source voltage decreases and if body effect increases (negative V_{bs}).

When low threshold voltage adder circuit is in standby mode all high threshold sleep nMOS and pMOS transistors N_1, N_2 and P_1 are turned off, due to this low V_{th} circuit disconnected from supply and ground and leakage current reduces. At the same time intermediate node V_{gnd2} is charged up to some positive potential due to some small drain current of sleep nMOS transistor N_1, the drain-to source potential V_{ds1} of sleep transistor N_1 reduces due to this intermediate node voltage V_{gnd2}, It causes less drain induced barrier lowering effect and negative body-to-source voltage V_{bs1} of sleep transistor N_1 leads to body effect. In this way stacking of transistor reduces sub threshold leakage in the circuit. The transistor N_2 is diode connected, when this diode is reverse biased, the source is seemed to be connected at gate, so drain to source voltage V_{ds} of transistor N_2 reduces and due to this reduction in V_{ds} of transistor N_2 the leakage current also reduces.

When circuit transition takes place from sleep to wait mode the sleep transistor P_1 turns on, but at the same time transistor N_1 and N_2 are in cut-off state. Forward body biasing is used on wait transistor P_1, due to which virtual ground V_{gnd1} discharges up to threshold voltage of P_1 transistor easily without increasing the width of transistor and the first peak of ground bounce noise, coming across it, will increase. To complete the reactivation cycle, transition of circuit goes from wait to active mode in which sleep transistor P_1 turns off and transistors N_1 and N_2 are turned on subsequently. By controlling the drain to source voltage of transistor N_2 and intermediate node voltage V_{gnd2} the ground bounce noise can be controlled more effectively. In wait to active mode transition the transistor N_1 turns on first, at this moment the capacitance C_1 starts charging. When the capacitor C_1 is charged up to the threshold value of transistor N_2 the transistor N_2 turns on and capacitor C_1 starts discharging. Hence the ground bounce noise reduces.

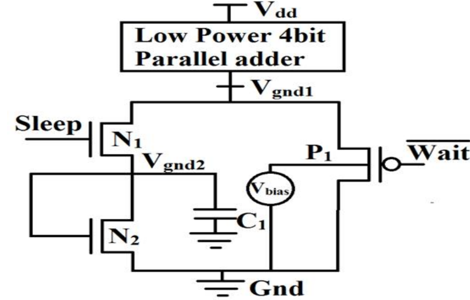

Fig.2. Diode Based trimode technique

III. Proposed Techniques

A. ULP Diode with parallel sleep pMOS transistor

ULP diode : In the proposed Power Gating technique the transistor P_2 and N_2 forms Ultra low power (ULP) diode as shown in (Fig.3) [6][10]. The transistors N_1, N_2, P_1, P_2 and P_3 are high threshold sleep pMOS and nMOS transistors. The sleep transistor N_1 is in series with ULP diode, used here to reduce the leakage and ground bounce noise as discussed in the previous section. The parallel sleep pMOS transistors P_1 and P_3 are used to add an extra wait state [8]. So there total three modes of operation sleep, wait and active.

Ultra low power diode is the combination of nMOS and pMOS transistors, which is used to reduce leakage current more effectively. The weak inversion drain current for nMOS and pMOS transistors are given by

$$I_{d,N_2} = I_{sno}e^{\frac{V_{gs,N_2}}{nV_T}}e^{\frac{\eta V_{ds,N_2}}{nV_T}}\left(1-e^{\frac{-V_{ds,N_2}}{V_T}}\right) \quad (3)$$

$$I_{d,P_2} = I_{spo}e^{-\frac{V_{gs,P_2}}{nV_T}}e^{\frac{\eta V_{ds,P_2}}{nV_T}}\left(1-e^{\frac{-V_{ds,P_2}}{V_T}}\right) \quad (4)$$

Where V_{gs} and V_{ds} are gate-to-source and drain-to-source voltage respectively, n is body coefficient, V_T = kT/q is the thermal voltage and η is drain induced barrier lowering (DIBL) coefficient. I_{sno} and I_{spo} are reference currents that correspond to the extrapolation of weak inversion drain current for V_{gs}=0 and V_{ds} in saturation (but low enough to neglect DIBL).

When the adder circuit is in standby mode, Ultra low power diode comes in reverse bias condition, and sleep transistor P_2 and N_2 are operating with negative gate to source voltage V_{gs}, it reduces the leakage current of the circuit. As

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given in equation (1) and (2) the leakage current is directly proportional to transistor width, if width (W) of transistor decrease, leakage also reduces. In proposed design uses two parallel wait sleep pMOS transistors P_1 and P_3, the width (W) of transistors P_1 and P_3, shown in (Fig.3) is half of the width of the transistor P_1 of (Fig.2). So by decreasing the W of transistor the leakage reduces here more effectively. To further reduce the Leakage current uses reverse body biasing on sleep pMOS transistors in standby mode. It increases the threshold voltage of the transistors, so leakage of the circuit reduces.

When low V_{th} circuit transition takes place from sleep to active mode, it will go from sleep to wait mode, at this time transistor P_3 turns on but sleep transistors N_1, N_2, P_1 and P_2 are turned off, at the same time virtual ground voltage V_{gnd1} discharges through P_3 up to the threshold voltage V_{tp3} of sleep transistor P_3. The first peak of ground bounce noise comes across it. The virtual ground voltage can be discharged easily by using forward body biasing (FBB) on sleep transistor P_3 without increasing the size of wait transistor [12]. After a small time second wait transistor P_1 turns on and forward body biasing is applied on it so again virtual ground voltage is discharged through it up to the amount of threshold voltage V_{tp1} of transistor P_1 and a second peak of ground bounce comes across it. The virtual ground can be discharged easily by using Forward body biasing on P_1 and P_3 sleep transistors. To complete the reactivation process the circuit goes from wait to active mode and transistor P_1 and P_3 turns off and transistor N_1 turns on, due to which capacitor C_1 starts charging. When capacitor is charged up to the threshold voltage of transistor N_2, the transistor N_2 turns on and capacitor C_1 starts discharging. In this way the use of transistor stacking, ultra low power diode and parallel pMOS sleep transistor 'P_3' and body biasing reduces the Ground bounce noise to a considerable amount.

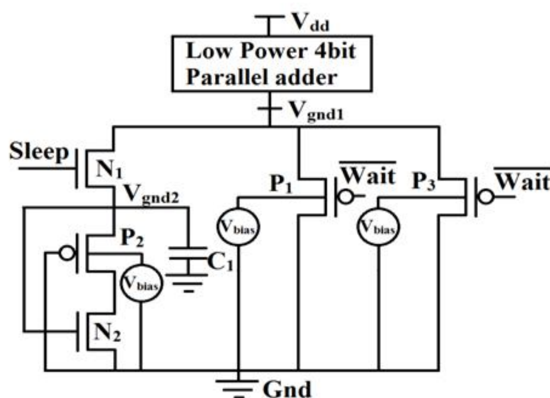

Fig.3. ULP Diode with parallel sleep pMOS transistor Proposed design

A. Single header based ULP Diode with parallel sleep pMOS transistor

In this proposed design transistor N_1, N_2, P_1, P_2, P_3 and P_4 are high threshold sleep transistors. Transistor P_2 and N_2 are making Ultra low power diode as shown in Fig.4, which works similar as discussed in the previous section. Transistor N_1 is connected in series to make stacking of transistor which is helpful to reduce the Leakage current as discussed in section II. Capacitor C_1 is used to control the intermediate node voltage V_{gnd2} and Ground Bounce Noise. An extra header sleep transistor is added here to reduce the leakage and the ground bounce noise of the system.

When circuit is in standby mode all sleep transistors P_1, P_2, P_3, P_4, N_1 and N_2 are turned off, the low V_{th} circuit disconnected from supply and ground and leakage reduces. At this time the intermediate node V_{gnd2} charge up to some positive potential due to small drain current of N_1 transistor, it reduces the drain to source voltage V_{ds1} of N_1 transistor and reduces leakage as shown in equation (1)(2). Due to stacking of transistor by using Ultra Low Power diode leakage reduces to a considerable amount as discussed in previous section. Here uses extra parallel sleep pMOS transistor P_1 and P_3, whose width (W) is half of the width of P_1 sleep transistor of Fig.2 and uses the reverse body biasing on sleep wait pMOS transistors P1 and P_3.the reverse body biasing increases the threshold voltage of the circuit and reduces. Due to reduction of transistor width and using reverse body biasing on sleep pMOS transistor in standby mode the leakage reduces to a considerable amount.

When circuit transition takes place from sleep to wait state, transistor P_4 and P_3 turn on, but other transistor P_2, N_1 and N_2 are in cut-off state, the Virtual V_{dd} node voltage reduces up to the threshold voltage P_4 sleep transistor (V_{dd}-V_{thp4}), and this voltage is discharge up to the threshold voltage of P_3 sleep transistor, due to this the first peak of ground bounce noise comes across P_3 transistor, after a small time P_1 transistor turns on and the virtual V_{dd} node voltage discharge up to the threshold voltage of P_1 transistor and second peak of ground bounce noise comes across it. To complete the reactivation process the transition takes place from wait to active mode in which transistor N_1, N_2 and P_2 are turns on and the third peak of Ground Bounce noise comes across it. By using forward body biasing and resizing of wait transistor size the ground bounce noise is further reduce to a considerable amount [12].

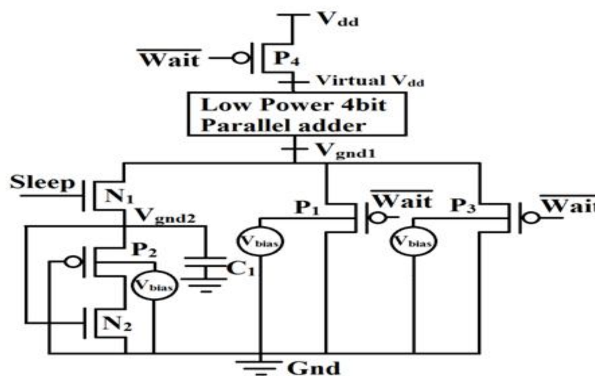

Fig.4. Single header based ULP Diode with parallel sleep pMOS transistor

IV. Simulation Result and Discussion

All simulation is done on four bit binary parallel adder circuit. The block diagram of four bit binary adder is shown

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in Fig.5. The basic circuit diagram of one bit full adder is shown in Fig.6.

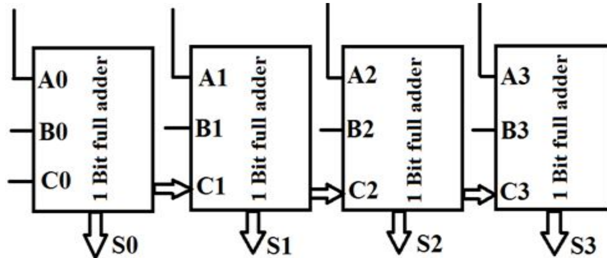

Fig.5 Four bit binary parallel adder block diagram

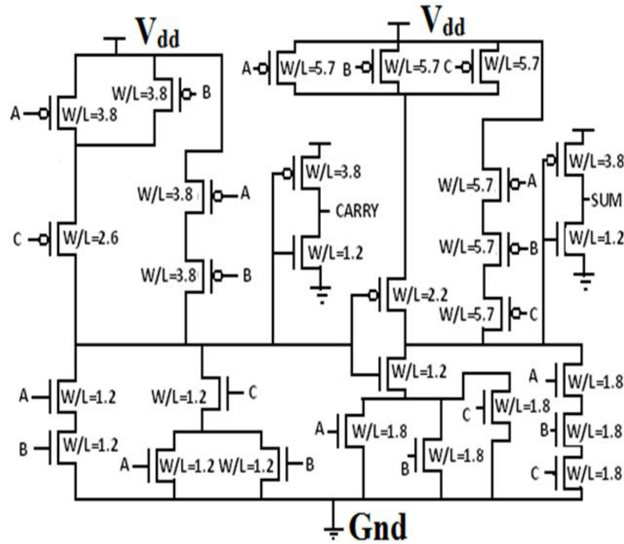

Fig.6. One bit adder circuit diagram

A. Leakage Analysis

Leakage analysis of the four bit binary adder circuit in standby mode is done in this section with different power gating techniques. Leakage analysis on different Body bias voltage on sleep transistors, for different supply voltage and temperature has been analyzed in this section.

TABLE I. LEAKAGE CURRENT ANALYSIS FOR DIFFERENT POWER GATING TECHNIQUE WITH CHANGE IN BODY BIAS VOLTAGE

Power Gating Technique	Leakage current with change in Body Bias voltage				
	1.4	1.2	1	0.8	0.6
Diode based trimode	1.47E-09	1.47E-09	1.48E-09	1.49E-09	1.54E-09
ULP Diode with parallel sleep pMOS transistor	2.73E-10	4.12E-10	6.21E-10	9.14E-10	1.25E-09
Single header based ULP Diode with parallel sleep pMOS transistor	2.68E-10	4.08E-10	6.17E-10	9.11E-10	1.35E-09

Table I shows the simulation results for four bit binary adder circuit for different power gating techniques. The result shows that the leakage current of the circuit increases, when applying forward body biasing on sleep transistors in sleep mode and reduces when applying reverse body biasing on sleep transistors in sleep mode.

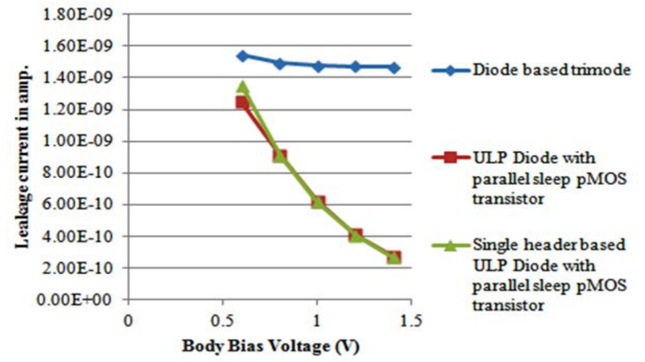

Fig.7. Leakage current analysis with change in body bias voltage

Fig.7 shows the leakage current comparison of four bit binary parallel adder circuit for different power gating techniques.

TABLE II. LEAKAGE CURRENT ANALYSIS FOR DIFFERENT POWER GATING TECHNIQUE WITH CHANGE IN SUPPLY VOLTAGE

Power Gating Technique	Leakage current with change in supply voltage				
	1.4	1.2	1	0.8	0.6
Diode based trimode	8.72E-08	5.34E-09	1.48E-09	1.10E-09	8.15E-10
ULP Diode with parallel sleep pMOS transistor	8.68E-08	4.76E-09	6.21E-10	4.56E-10	3.46E-10
Single header based ULP Diode with parallel sleep pMOS transistor	8.68E-08	4.76E-09	6.17E-10	4.62E-11	2.07E-13

Table II shows the leakage current simulation result for four bit full adder circuit for different power gating techniques with change in supply voltage, it shows that with supply voltage scaling the leakage current of the circuit also reduces.

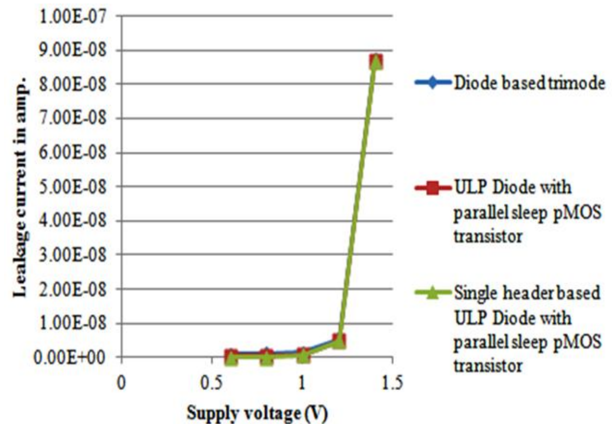

Fig.9.Leakage current analysis for different power gating technique with temperature

B. Ground Bounce Noise analysis

When the Power gating MTCMOS circuit transition takes place from sleep to active mode there is a sudden discharge path from supply to ground as shown in Fig.1, so due to this a sudden discharge surge current comes from supply to ground, which disturbs the circuit output transition to a wrong output, this noise is called Ground bounce noise. Ground

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bounce noise for different body bias voltage on parallel sleep wait pMOS transistors, for different size of wait pMOS transistors, for different temperature, for different supply voltage has been analyzed in this section. For modelling ground bounce noise for different power gated circuit the electrical characteristics of 40 pin dual in line package (DIP-40) package model has been used as shown in Fig.10.

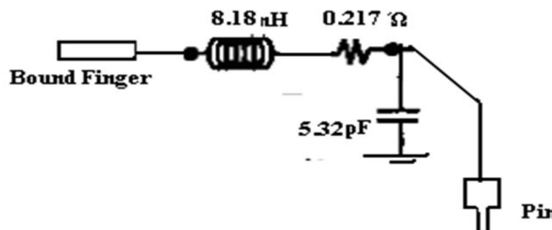

Fig.10.DIP -40 Package Pin Ground Bounce Noise Model

TABLE IV. GROUND BOUNCE NOISE ANALYSIS FOR DIFFERENT POWER GATING TECHNIQUE WITH CHANGE IN BODY BIAS VOLTAGE

Power Gating technique	GBN in mv with change in Body Bias voltage				
	1.4	1.2	1	0.8	0.6
Diode based trimode	1.65	1.71	1.75	1.78	1.8
ULP Diode with parallel sleep pMOS transistor	1.52	1.55	1.57	1.58	1.59
Single header based ULP Diode with parallel sleep pMOS transistor	1.46	1.48	1.50	1.51	1.52

The table IV shows the simulation results of ground bounce noise for four bit binary adder power gated circuit. The result shows that by applying forward body biasing on sleep wait transistor P_1 and P_3 the ground bounce noise peak through theses sleep transistor increases.

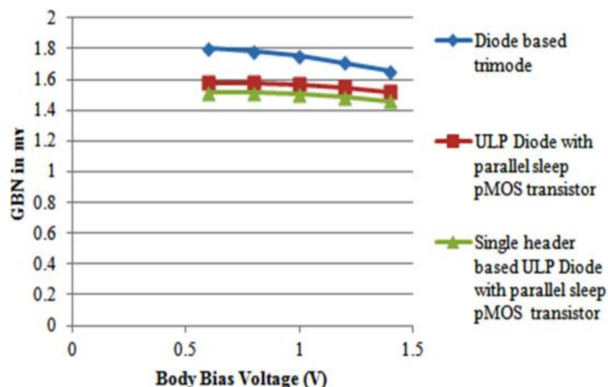

Fig.11.Ground Bounce Noise (GBN) analysis with change in body bias voltage

The Ground Bounce noise analysis with change in body bias voltage on parallel sleep pMOS transistors P_1 and P_3 for different power gating circuit is shown in Fig.11.

Table V shows the simulation results of ground bounce noise for four bit binary adder circuit with change in size of wait sleep transistor P_1 and P_3 of different power gating techniques. It shows that as the size of wait transistor increases the peak of ground bounce noise also increases.

Fig.12 shows the ground bounce analysis for different power gating techniques with change in wait transistor size.

TABLE V. GROUND BOUNCE NOISE ANALYSIS FOR DIFFERENT POWER GATING TECHNIQUE WITH CHANGE WAIT TRANSISTOR SIZE

Power Gating technique	GBN in mv with change in size of parallel sleep pMOS Transistor					
	1	3	6	9	13	15
Diode based trimode	1.17	1.2	1.39	1.52	1.68	1.75
ULP Diode with parallel sleep pMOS transistor	0.9	1.27	1.49	1.64	1.83	1.92
Single header based ULP Diode with parallel sleep pMOS transistor	0.88	1.23	1.43	1.57	1.73	1.80

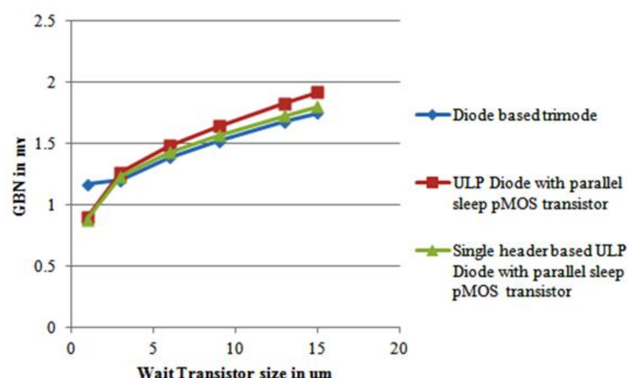

Fig.12.Ground Bounce Noise (GBN) analysis with change in wait transistor size

TABLE VI. GROUND BOUNCE NOISE ANALYSIS FOR DIFFERENT POWER GATING TECHNIQUE WITH CHANGE IN TEMPERATURE

Power Gating technique	GBN in mv with change in Temp		
	25	45	65
Diode based trimode	1.752	1.772	1.798
ULP Diode with parallel sleep pMOS transistor	1.57	1.58	1.59
Single header based ULP Diode with parallel sleep pMOS transistor	1.5	1.52	1.54

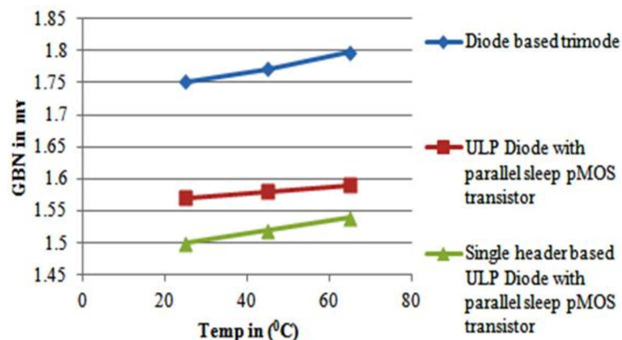

Fig.13.Ground Bounce Noise (GBN) analysis with change in temperature in ^{0}C

Table VI shows the simulation results of ground bounce noise for four bit binary adder circuit for different power gating techniques with change in temperature. The result shows that the Ground bounce Noise increases with increases in temperature.

The Ground bounce analysis with change in temperature is shown in Fig.13 for different power gating techniques.

Table VII shows the simulation results of ground bounce noise for different power gating techniques, for four bit

binary parallel adder circuit with change in supply voltage. The simulation results on the four bit binary power gating adder circuit shows that the ground bounce noise of the circuit increases with increases in supply voltage and decreases with reduction in supply voltage.

TABLE VII. GROUND BOUNCE NOISE ANALYSIS FOR DIFFERENT POWER GATING TECHNIQUE WITH CHANGE IN SUPPLY VOLTAGE

Power Gating technique	GBN in mv with change in supply voltage				
	1.4	1.2	1	0.8	0.6
Diode based trimode	1.88	1.84	1.75	1.16	0.71
ULP Diode with parallel sleep pMOS transistor	2.08	1.85	1.57	1.17	0.66
Single header based ULP Diode with parallel sleep pMOS transistor	2.03	1.58	1.50	0.53	0.35

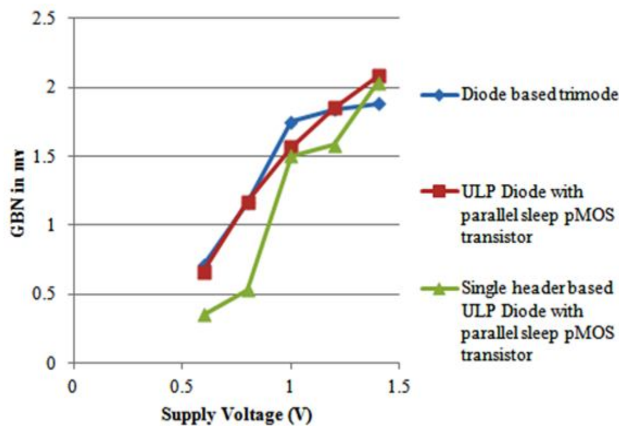

Fig.14.Ground Bounce Noise (GBN) analysis with change in supply voltage

The ground bounce noise analysis with change in supply voltage is shown in Fig.14.

V. FURTHER REDUCTION OF GROUND BOUNCE

By applying FBB and transistor resizing on “single header based ultra low power diode with parallel sleep pMOS transistor” the ground bounce noise can be further reduced [17][18].

When the wait transistor size of P_1=7.5um and P_3=7.5 um and body bias voltage is 1V in “Single header based Ultra Low Power diode with parallel sleep pMOS transistor” the first, second peak (during sleep to wait mode transition) and third peak (during wait to active mode transition) of ground bounce noise is shown in Fig.15 and voltage corresponding to the peak are 1.505mv, 1.3525mv and 1.1126mv as shown in table VIII.

To further reduce the peak of ground bounce noise applying forward body biasing (V_b=0.8V) on sleep parallel wait transistors P_1 and P_3. In this way from sleep to wait mode transition the first peak and the second peak voltage of Ground bounce noise increases here as shown in Fig.16 and corresponding values 1.5147mv and 1.4321mv, and the third peak of ground bounce noise from wait to active mode transition reduces up to the voltage 1.0957mv.

To further reduce the ground bounce noise, resizing the wait transistor up to width of (P_1=6um and P_3=6um). By reducing the wait transistor size the peak of ground bounce noise across it reduces as already discussed in section. Which is shown in Fig.17, from sleep to wait mode transition the first peak and the second peak of ground bounce noise reduces up to 1.441mv and 1.3423mv respectively and the third peak voltage reduces up to 1.08mv from wait to active mode transition. To further reduction of ground bounce noise peak again resize the wait transistor size up to width of (P_1=4um and P_3=4um), it will further reduce the ground bounce noise first and second peak up to 1.33mv and 1.19mv during sleep to wait mode transition and third peak up to1.058mv during wait to active mode transition as shown in Fig.18 and table VIII.

Table VIII. Ground Bounce Noise Peaks for different wait transistors size and body bias voltage

Body bias Voltage in V	Wait transistor size		Peaks of GBN in mv		
			Peak1	Peak2	Peak3
BB=1	W_1=7.5um	W_2=7.5um	1.51	1.35	1.11
BB=0.8	W_1=7.5um	W_2=7.5um	1.51	1.43	1.09
BB=0.8	W_1=6um	W_2=6um	1.44	1.34	1.08
BB=0.8	W_1=4um	W_2=4um	1.33	1.19	1.06
BB=0.8	W_1=1.4um	W_2=2.5um	1.03	1.03	1.03

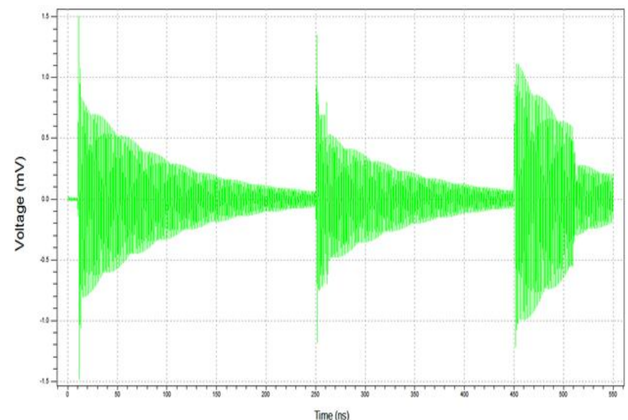

Fig.15.Ground Bounce Noise analysis with wait transistor size (W_{P1}=7.5um and W_{P3}=7.5um) and body bias voltage (V_b=V_{dd}=1V)

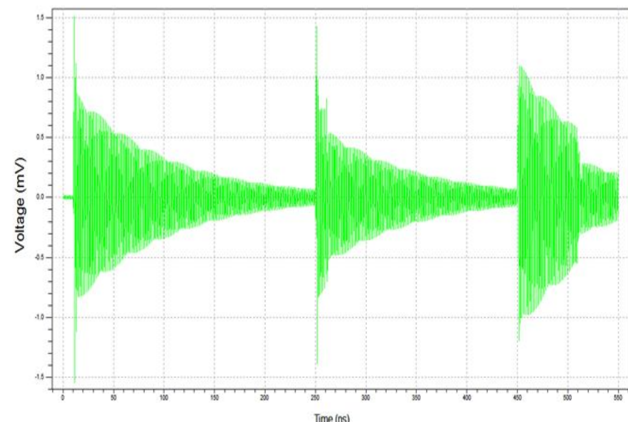

Fig.16.Ground Bounce Noise analysis with wait transistor size (W_{P1}=7.5um and W_{P3}=7.5um) and body bias voltage (V_b=0.8V)

To further reduce the peak of ground bounce noise try to make such type of combination of wait transistor size so that the all three peaks of ground bounce noise become equal in amplitude as shown in Fig.19. In this case the Ground bounce noise comes minimum in comparison to all other cases. For this again resize the wait transistor size of P_1 and P_3 up size of (P_1=1.4um and P_3=2.5um). At this combination of body biasing and transistor size the all three peaks of ground bounce noise from sleep to wait mode and wait to active mode transition of the circuit become equal in amplitude that is 1.0287mv.

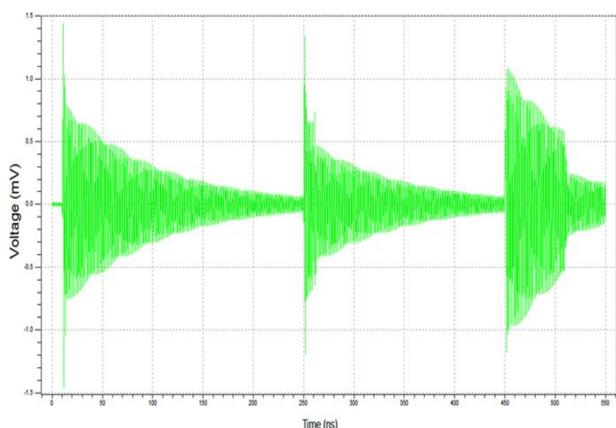

Fig.17.Ground Bounce Noise analysis with wait transistor size (W_{P1}=6um and W_{P3}=6um) and body bias voltage (V_b=0.8V)

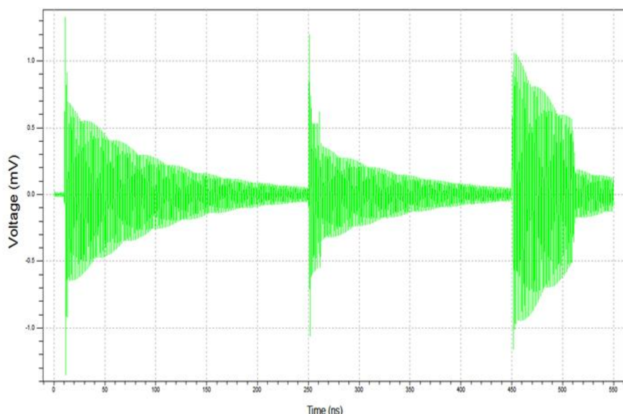

Fig.18.Ground Bounce Noise analysis with wait transistor size (W_{P1}=4um and W_{P3}=4um) and body bias voltage (V_b=0.8V)

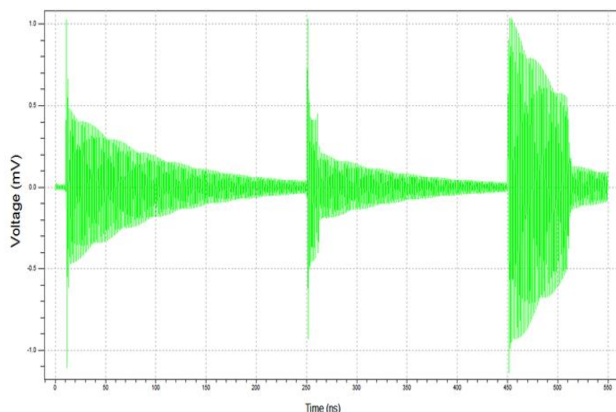

Fig.19.Ground Bounce Noise analysis with wait transistor size (W_{P1}=2.5um and W_{P3}=1.4um) and body bias voltage (V_b=0.8V)

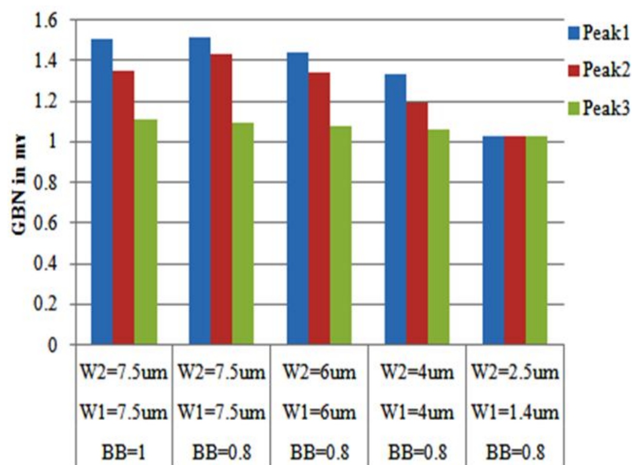

Fig.20.Ground Bounce Noise analysis with wait transistor size W_{P1} and W_{P3} and body bias voltage V_b

Fig.20 shows the Ground bounce noise comparison for first, second and third peaks. It shows that all peaks of ground bounce noise become equal in amplitude at wait transistor size W_{P1}=1.4um and W_{P3}=2.5um at 0.8V body bias voltage.

VI. Conclusion

Leakage current reduction in standby mode and Ground bounce noise reduction during mode transition for diode based trimode technique, Ultra Low Power diode with parallel sleep pMOs transistor with body biasing and Single header based Ultra Low Power diode with parallel sleep pMOs transistor with body biasing has been evaluated in this paper. Use of transistor stacking, forward body biasing, reverse body biasing, ultra low power diode and wait transistor resizing reduces ground bounce noise and leakage current to a considerable amount. Effect of wait transistor resizing, temperature, body biasing on sleep transistor and supply voltage on leakage and ground bounce noise have been analyzed in this paper.

It has been observed that by using proposed design "Ultra Low Power diode with parallel sleep pMOS transistor with body biasing" and "Single header based Ultra Low Power diode with parallel sleep pMOS transistor with body biasing" Leakage can be reduces up to 70.40% and 70.70% respectively by using reverse body biasing in comparison to Diode based trimode technique and Ground bounce Noise can be reduced by to 10.38% and 14.02% respectively in comparison to "Diode based trimode technique". With increment of temperature and supply voltage the peaks of ground bounce noise and leakage current increases. By reducing the wait transistor size the ground bounce noise peak further reduces.

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