Proceedings of the SMART–2021, IEEE Conference ID: 52563
10th International Conference on System Modeling & Advancement in Research Trends, 10th–11th December, 2021
Faculty of Engineering & Computing Sciences, Teerthanker Mahaveer University, Moradabad, India

2021 10th International Conference on System Modeling & Advancement in Research Trends (SMART) | 978-1-6654-3970-1/21/$31.00 ©2021 IEEE | DOI: 10.1109/SMART52563.2021.9676257

Performance Analysis and Characterization of Double Gate and Gate All Around MOSFET

Yusra Siddiqui[1], Nupur Mittal[2], Imran Ullah Khan[3]*
[1,2,3]Department of ECE, Integral University,Lucknow, India
E-mail: [1]yusraiu@student.iul.ac.in, [2]mittal@iul.ac.in, [3*]iukhan@iul.ac.in

Abstract—**The optimization and comparison of structure of double-gate MOSFETs and gate-all-around (GAA) MOSFETs was carried out. The fin width to gate length ratio and SCE (short channel effects) were discussed and studied. The 3-D simulations affirmed that while gate length was same as fin width, the short channel effects were inhibited. The ratio of the fin width to the gate length was maximized up to 1.2 in cylindrical channel GAA MOSFETs as compared to cubical channel ones.**

Keywords: MOSFET, GAA, Short Channel Effects, DIBL and Silvaco TCAD

I. Introduction

In CMOS for the sub-50-nm regime, Double-Gate (DG) MOSFETs, owing to good short-channel-effect (SCE) immunity and high transconductance, have been regard as most optimistic choice [1]. The ratio of fin width to the gate length is considered to be crucial design parameters, in order to have better DIBL (drain-induced barrier lowing) and SS (sub threshold swing) [2]. For proper inhibition of SCEs, fin width found to be 0.7 times less than the gate length [3]. Hence, fin width being the most crucial factor in determining the critical dimension, stands as a hindrance to aggressive scaling. The gate electrodes and the gate oxide envelop around the channel region in GAA (Gate All Around) MOSFETs. Fin width to the gate length ratio is increased while using GAA MOSFETs. Since the gate length is smaller than fin width, the SCEs are sufficiently minimized, if the design variable of GAA MOSFETs are optimized. In this work, double gate MOSFET and Gate All Around MOSFETs were quantitatively investigated by ratio of fin width to the gate length optimely. Initially, 30-nm DG and GAA MOSFET structures are introduced [4].

Multiple gate lengths, gate-oxide thickness, fin heights and fin widths were used to perform three dimensional simulations for DG and GAA MOSFETs to analyze short channel effects. Based on the results, the design optimization of GAA MOSFET was focused and was established that the GAA MOSFETs were optimized with cubical channel where all three parameters fin width, fin height and gate length were all equal [12-14].

II. Different Gate Structures

Short-channel effects appear when gate control is affected by electric field lines between drain and source [5]. Increasing the doping concentrations of the channel can minimize the effects of electric field lines that propagate through depletion regions, in a bulk device (figure 3A). However, as a result of large doping concentrations the proper functioning of small devices is hindered. Before reaching the channel majority of electric field lines, in FDSOI devices, go through buried oxide layer (Fig. 3B). By using thin BOX and ground plane under it, SCEs in FDSOI MOSFETs can be minimized (figure 3C). Increased junction capacitance and increased body effect, are the major drawbacks of the approach [6-10]. The electric field lines terminate at the bottom gate electrode in a double gate structure; hence a greater competent device structure is achieved. Figure 1 shown the different Gate structures. Equations 1 to 4 indicate DIBL and short channel effects in FDSOI and double gate.

FDSOI Drain Induced Barrier Lowering =

$$0.80[\varepsilon_{si}/\varepsilon_{ox}\ \{(1+t_{si}^2/L_{el}^2)t_{ox}/L_{el}(t_{si}+\lambda t_{BOX}/L_{el})\}V_{DS}] \quad (1)$$

FDSOI Short Channel Effects =

$$0.64[\varepsilon_{si}/\varepsilon_{ox}\ (1+t_{si}^2/4L_{el}^2)t_{ox}/L_{el}\{(t_{si}+\lambda t_{BOX}/L_{el})\}V_{bi}] \quad (2)$$

DG Drain Induced Barrier Lowering =

$$0.80[\varepsilon_{si}/\varepsilon_{ox}\ \{(1+t_{si}^2/L_{el}^2)t_{ox}/L_{el}(t_{si}/2L_{el})\}V_{DS}] \quad (3)$$

DG Short Channel Effects =

$$0.64[\varepsilon_{si}/\varepsilon_{ox}\ \{(1+t_{si}^2/L_{el}^2)t_{ox}/L_{el}(t_{si}/2L_{el})\}V_{bi}] \quad (4)$$

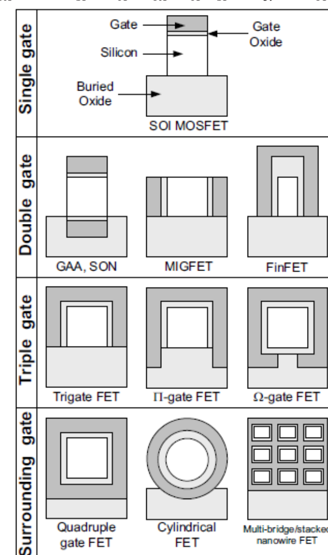

Fig. 1: Different Gate Structures

Copyright © IEEE–2021 ISBN: 978-1-6654-3970-1

Authorized licensed use limited to: DRDO-CABS. Downloaded on May 18,2022 at 03:45:28 UTC from IEEE Xplore. Restrictions apply.

III. Result and Discussion

A. Optimization of GAA MOSFETs

Simulations for various gate-oxide- thickness and Fin height splits were conducted to optimize GAA MOSFETs' design parameters and reduce short-channel. Simulations were performed for1.5, 2, 2.5, and 3 nm gate-oxide thicknesses in the beginning.

It was observed that in both the devices, with reduction in the gate-oxide thickness DIBL gradually decreased. Taking into account the obstacles, the optimal gate-oxide thickness is set to 2 nm in the fabrication process. Even for the 30 nm Fin width, in case of gate oxide thickness of 2-nm, the DIBL stayed below 115 mV/V, as shown in Fig. 5. an additional notable thing in fig 6 was that in GAA MOSFETs, with 3-nm thick gate-oxide, the SS and DIBL characteristics were superior compared to 2nm thick gate oxide in DG MOSFETs. Thus, showing that, in respect of CMOS scaling GAA MOSFETs have an advantage. Fig. 8 shows DIBL and SS characteristics for 30, 35, 40, 45, and 50 nm fin heights, for both devices. The reduction in fin height resulted in improved SS and DIBL for GAA MOSFETs but remained same for DG MOSFETs. In case of GAA MOSFETs, due to increased controllability, owing to additional gates on the channel, reduction in fin height resulted in reduction of short channel effects. For relevant SS and DIBL, it was confirmed from the data, fin width can be same or larger than gate length.

B. Ideal Cylindrical-Channel MOSFETs

The design was optimized for GAA MOSFETs, as the gate length, the fin height, and the fin width were taken as 30 nm, and gate oxide thickness was 2nm, for proper inhibition of SCEs in previous simulation results. As a consequence, the GAA MOSFETs' performance had been improved with a cubical channel. DG MOSFETs generally do not suffer corner effects like GAA MOSFETs generally do. Reliability problem and the short-channel effects may arise, as the large electric field accumulate around each channel edges, thus channel cannot be evenly controlled by gates.

Summary of results is illustrated in Table 1-4. In the cubical-channel MOSFETs the electric fields are out of balance unlike ideal cylindrical channel MOSFET, where the gate electric field equally affects the channels, and hence OFF currents are notably reduced. Improvement of driving current was likely as the channel volume is enhanced that would lead to higher current flow. Due to increase in SS, OFF current became worse. DIBL and SS characteristics are shown in fig 12 with cylinder diameters. As it could be anticipated that cylinder diameter increase could cause the SS and DIBL to rise. In Fig 4 and 5, 84.8 mV/dec and 118.38 mV/V were the values of the SS and DIBL respectively.

Short channel effects were still minimized even when the gate length is smaller than cylinder diameter. For pertinent short channel effect, proportion of the cylinder diameter to the gate length could be increased to 1.2. Table 1-4 gate voltage vs g_m, gate length vs threshold voltage, Fin width vs Sub Threshold Swing characteristics and Fin width vs Drain Induced Barrier Lowering respectively. Figure 2-5 shows characteristics based on values obtained in table 1 to 4.

Table. 1: Gate Voltage vs Transconductance for Double Gate and Gate All Around Structure

S.No.	Gate Voltage (Volt)	Transconductance (g_m) (mS/µm)	
		g_m for DG	g_m for GAA
1.	-1	0	0
2.	-0.8	0	0
3.	-0.6	0	0
4.	-0.5	0	0
5.	-0.3	0	0
6.	-0.1	0.02	0.02
7.	0	0.04	0.04
8.	0.1	0.05	0.06
9.	0.3	0.06	0.09
10.	0.5	0.03	0.04
11.	0.6	0.02	0.03
12.	0.8	0.01	0.02
13.	1	0.01	0.02

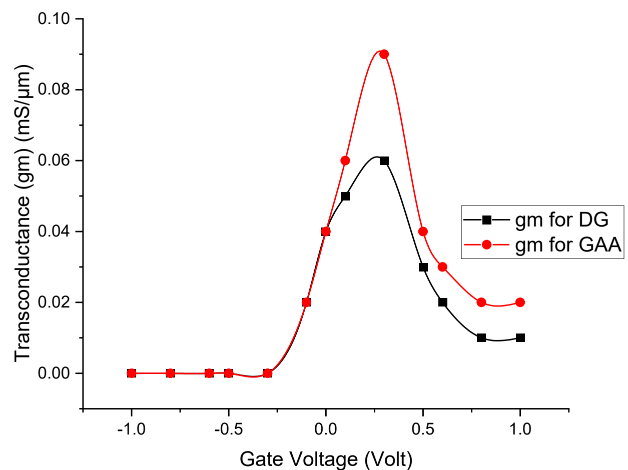

Fig. 2: Gate Voltage vs Transconductance for Double Gate and Gate All Around Structure

Copyright © IEEE–2021 ISBN: 978-1-6654-3970-1

Authorized licensed use limited to: DRDO-CABS. Downloaded on May 18,2022 at 03:45:28 UTC from IEEE Xplore. Restrictions apply.

TABLE. 2: GATE LENGTH VS THRESHOLD VOLTAGE

S.No.	Gate Length (nm)	Threshold Voltage (Volt)	
		DG	GAA
1.	10	-0.215	-0.18
2.	20	-0.2	-0.16
3.	30	-0.18	-0.15
4.	40	-0.16	-0.15
5.	50	-0.15	-0.147
6.	60	-0.148	-0.146
7.	70	-0.146	-0.144
8.	80	-0.142	-0.14
9.	90	-0.14	-0.138
10.	100	-0.14	-0.135

TABLE. 3: FIN WIDTH VS SUB THRESHOLD SWING CHARACTERISTICS

S. No.	Fin Width (nm)	Sub Threshold Swing			
		DG (t_{ox}=2nm)	DG (t_{ox}=3nm)	GAA (t_{ox}=2nm)	GAA (t_{ox}=3nm)
1.	10	64	65	62	64
2.	12	64	66	63	65
3.	15	70	72	68	70
4.	18	72	77	70	72
5.	20	75	80	71	74
6.	23	77	85	74	76
7.	25	80	90	76	78
8.	28	82	97	78	80
9.	29	84	99	80	82
10.	30	90	105	82	88

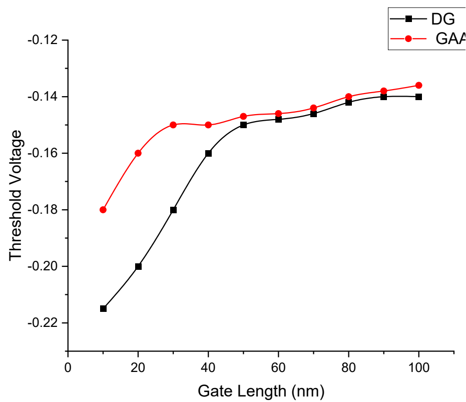

Fig. 3: Gate Length vs Threshold Voltage for Double Gate and Gate All Around Structure

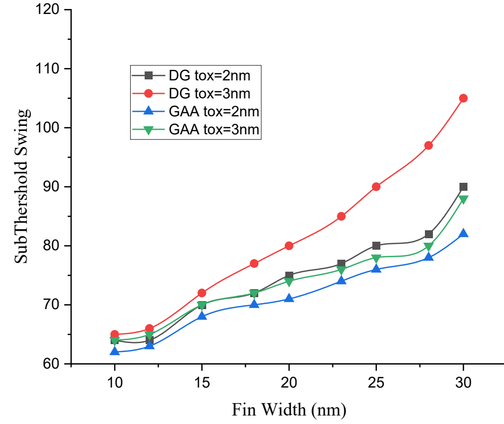

Fig. 4. Fin Width vs Sub Threshold Swing Characteristics for Double Gate and Gate All Around structure for Different t_{ox}

Drain Induced barrier Lowering (DIBL) = $\Delta V_{Th}/\Delta V_{DS}$

$=(V_{Th1} - V_{Th2})/(V_{DS1} - V_{DS2})$

ΔV_{Th} = Threshold Voltage

ΔV_{DS} = Drain to source voltage

TABLE. 4: FIN WIDTH VS DRAIN INDUCED BARRIER LOWERING

S. No.	Fin Width (nm)	Drain Induced Barrier Lowering (mV/V)			
		DG (t_{ox}=2nm)	DG (t_{ox}=3nm)	GAA (t_{ox}=2nm)	GAA (t_{ox}=3nm)
1.	10	29	32	20	28
2.	12	41	48	25	40
3.	15	49	59	34	48
4.	18	52	65	45	51
5.	20	60	77	50	56
6.	23	80	90	52	65
7.	25	92	115	60	70
8.	28	105	130	68	82
9.	29	120	180	76	86
10.	30	140	240	80	95

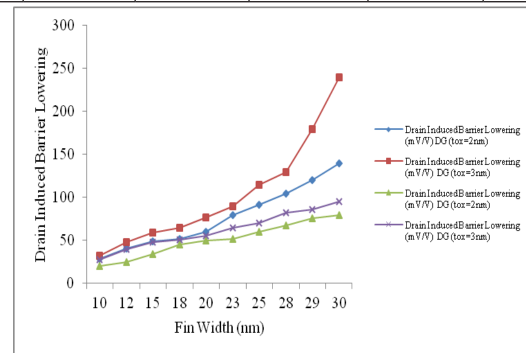

Fig. 5: Fin width vs Drain Induced Barrier Lowering for Double Gate and Gate All Around Structure for Different t_{ox}

Copyright © IEEE–2021 ISBN: 978-1-6654-3970-1

Authorized licensed use limited to: DRDO-CABS. Downloaded on May 18,2022 at 03:45:28 UTC from IEEE Xplore. Restrictions apply.

IV. Conclusion

The cylindrical-channel MOSFETs', simulations were performed. The Ideal cylindrical-channel MOSFETs with reduced corner effects compared to cubical-channel GAA MOSFETs had smaller SS and DIBL. Hence, it was observed that the cylindrical-channel could be employed for optimized GAA MOSFET structure and the short-channel effects were suppressed. However, the gate length is smaller than fin width in this ideal cylindrical-channel MOSFET with 1.2 as the maximum ratio of the fin width to the gate length.

References

[1] Kosmani, N.F; Fatimah, A.H; Razali, M.A;A comparison of performance between double-gate and gate-all-around nanowire MOSFET, Indonesian Journal of Electrical Engineering and Computer Science, vol. 13, No. 2, February 2019, pp. 801~807.

[2] J. Colinge, M. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, "Silicon-on-insulator gate-all-around device'," in Tech. Dig. IEDM, 2016, pp. 595–598.

[3] D. S.Woo, B. Y. Choi,W.Y. Choi, M.W. LEE, J. D. Lee, and B.-G. Park, "30 nm self-aligned FinFET with large source/drain fan-out structure," Electron. Lett., vol. 39, pp. 1154–1155, Jul. 2003.

[4] A. Ortiz-Conde, F. J. Garcia Sanchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," Microelectron. Reliabil., vol. 47, pp. 1953–1958, Nov. 2003.

[5] S. Johansson, E. Memisevic, L.-E. Wernersson and E. Lind, "High- Frequency Gate-All-Around Vertical InAs Nanowire MOSFETs on Si Substrates", IEEE Electron Dev. Lett., vol. 35, no. 5, pp. 518-520, May 2014.

[6] Q. Xu, J. Luo, H. Zhou, J. Niu, Q. Liang and C. Zhao, "Performance Breakthrough in Gate-All-Around Nanowire n- and p-Type MOSFETs Fabricated on Bulk Silicon Substrate", IEEE Trans. Electron Dev., vol. 59, no. 7, pp. 1885-1890, July 2012.

[7] Zhang, Y; Han, K; and Jiawei, L; A Simulation Study of a Gate-All-Around Nanowire Transistor with a Core–Insulator Micromachines, MDPI 2020, 11, 223, 1-12.

[8] Jena, B; Ramkrishna, B. S.; Dash, S. and Mishra, G. P. "Conical surrounding gate MOSFET: A possibility in gate-all-around family," Adv. Nat. Sci. Nanosci. Nanotechnol., vol. 7, no. 1, 2016.

[9] Singh, J.; Kumar, M.J. A planar junctionless FET using sic with reduced impact of interface traps: Proposal and analysis. IEEE Trans. Electron Devices 2017, 64, 4430–4434.

[10] X. Liang and Y. Taur, "A 2-D analytical solution for SCEs in DG MOSFETs," IEEE Trans. Electron Devices, vol. 51, no. 9, pp. 1385–1391, Sep. 2004.

Copyright © IEEE–2021 ISBN: 978-1-6654-3970-1

Authorized licensed use limited to: DRDO-CABS. Downloaded on May 18,2022 at 03:45:28 UTC from IEEE Xplore. Restrictions apply.